

SELECTING PCB SUPPLIERS

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OBJECTIVE

The objective of the PCB supplier selection process is to choose PCB suppliers (fabricators) that are capable of reliably supplying prototype and production quantity PCBs of the types being used in a product at competitive prices. In addition, it is important to choose suppliers capable of providing vital front-end design engineering support in areas such as material selection, design for manufacturability, lamination and plating.

A crucial part of this process is balancing the risks against the costs. Often, suppliers are chosen based on the price of the PCB on the purchase order rather than the cost of ownership of that same PCB. The cost of a PCB includes the cost of assembly, rework, test, repair, scrap, replacement, if defective, and field service costs. **It is rare that the lowest price PCB bid turns out to be the lowest cost.**

It is vital to choose fabricators who can keep the risk of failed prototype and production PCBs to the absolute minimum. Remember, a failed PCB costs a company, not only its cost, but also the cost of all the components mounted on it as well as a large quantity of troubleshooting labor. During prototyping, this cost includes the cost of project delay and delay in time to market. These costs overshadow all of the other costs related to bad PCBs. The PCB itself should never be the reason a PCB assembly is scrapped. If this happens, the PCB fabricator selection process has failed.

PCB fabricators who bid on a particular PCB are rarely equally capable of building the PCB. Worse, it is usually impossible to discern the relative capability of each from the information supplied by the sales activity.

Similarly, it is not likely that contract manufacturers, whose strengths are assembly and material management, will possess the technical capability to determine which PCB fabricators will make the best suppliers. As a result, the choices of fabricators that a CM can use must be supervised with the same vigilance that is used when assembly is done in house. **PCB fabricator approval must not be allowed to rest solely in the hands of the contract manufacturer.**

THE PCB FABRICATION SUPPLIER BASE

The complexity of PCBs ranges from small single sided on paper laminate with punched holes like those used in remote controls built by the million at the "simple" end. At the "complex" end are large panels with dozens of layers using high performance laminates built in relatively small quantities such as those used in super computers and high performance networking products. The spectrum of PCBs also includes flexible circuits.

As might be expected, fabricators have evolved who specialize in each of these areas. Fabricators good at one end of the complexity range tend not to be good at the other end. The trick in selecting a fabricator is to match its business model, manufacturing tooling and processes, materials inventory and technical expertise to the PCB types that are to be made by it. Implied in this statement is the need to accurately understand the characteristics of each PCB and to understand what characteristics of each fabricator candidate best match its needs. Also implied is that the characteristics of each PCB supplier needs to be understood. This latter is often aggravated by the fact that PCB sales people often don't know the limits of their factory well enough to make sure the PCB in question matches the capability of the fabrication shop. There is an old saw "The difference between a used car salesman and a computer salesman- the car salesman knows when he is lying to you". This, all too often, applies to PCB salesmen or their reps. Further, there are always a few commission driven sales people who will take orders that don't fit, just to make a sale. Luckily, these are rare.

There is a mindset in much of the PCB fabrication industry that “we’ll try anything”. When a try fails, the response is often that the PCBs will be remade free or no charges will be made. This is a way for a fabricator to extend its reach into new technology areas. However, it is always done at the expense of the customer. Such failures are never free. They always carry with them schedule hits while the PCB is remade. This cost can easily be the cost to operate the design team while replacement PCBs are made. Actually, the cost is usually much higher as the delay often translates to delayed time to market- the real schedule and cost driver.

Many fabricators willingly build prototypes that cannot be manufactured in volume due to excessively tight tolerances or reliance on process steps that don’t scale to volume. Often, the customer doesn’t know this until it is time to scale up volumes. Examples of this are two traces between pin routing on 1mm pitch BGAs and 8 mil holes on thick PCBs. As this is being written, there are PCBs being built for multi-gigabit products that are failing as a result of this kind of prototyping. It is imperative that this “cowboy” mentality be spotted before committing a product to a new technology. One way to do this is to look for examples of the proposed technology in volume manufacture. The author always looks for examples of PCBs of the type being considered passing through the production process during the survey.

Once a new fabricator has demonstrated the capability to build the PCBs in question, the safe approach to adding that supplier to the approved supplier list is to have a trial set of PCBs built that are not in the critical path of any project. Examples of this are splitting a production order with an already approved supplier, so that if anything goes wrong there will still be some good PCBs to work with.

One of the biggest differentiators among fabricators is the skill of the people running the operation. It has long been known that good, skilled people can make superior PCBs, even with the poorest of equipment. The reverse is not true. The fact that a fabricator has the most advanced equipment available or the best process control system doesn’t guarantee good PCBs.

On top of everything else, many fabricators are made up of several plants scattered over a wide geographic area, sometimes global. Nearly always, these plants are acquired by purchasing existing companies. Normally, the capabilities of each plant will be different. Some will be good at high complexity PCBs while others will be capable of only low complexity PCBs. Still others may be chartered to build complex PCBs when their capability is limited to low complexity PCBs. With fabricators of the multi-plant type, it is likely that only some of the plants or perhaps only one will be capable of manufacturing PCBs of the type being considered. If this is so, it is important to restrict **in writing** the manufacture of the PCB to only that plant. Failing to do this can result in the manufacture of the PCB being shifted to a less than capable plant. All too often this shift is only discovered when the yields after assembly drop to an undesirable level.

RISKS ASSOCIATED WITH INCORRECT FABRICATOR SELECTION

There are a number of ways that a PCB can turn out bad. The simplest is that the bare PCB costs too much. This is the result of selecting a fabricator whose processes are more robust and complex than the PCB warrants. This is the easiest, lowest cost problem that results from improper fabricator selection. It is also the easiest to fix. Just select a fabricator whose processes are just good enough to yield a PCB of the required quality.

The following types of failures can result from improper fabricator selection. Vias and plated through holes fail creating open circuits. Solder joints fail as a result of poor surface finishes. Shorts can be present in the PCB when it is new or grow due to metal migration. Opens can be present in a PCB when it is new or occur due to metal fatigue. Impedance can be the wrong value for a variety of reasons. The PCB may fail HIPOT testing due to leakage caused by contamination.

The failures in the second category are the most insidious. The reason is they usually don’t show up until the PCB has been assembled. Often, they are never found. The PCB sits in a “dog box” on the manufacturing floor because no one can fix it or it goes out to a customer and fails there. Very few manufacturers have the failure analysis and failure-tracking systems in place that can isolate these kinds

of failures well enough to trace them back to the PCB fabricator. As a result, bad PCBs are purchased for much longer than they should be.

It is these risks that make PCB fabricator selection such an important part of the supplier evaluation process. Sadly, the lack of visibility of these kinds of failure leads to the assumption that price is the only selection criteria for a PCB fabricator. As Ruskin points out, the common law of business states that you cannot pay a little and get a lot. If a PCB fabricator quotes a price noticeably lower than its competitors, odds are it is because of shortcuts, not superior skill. In which case, it is wise to set aside a reserve for the likelihood of PCBs being bad. When the reserve is large enough to cover the risk, it will amount to more than the potential savings. Said another way, beware the low bidder in a bidding group of equals.

Another reason for an excessively low bid is the deliberate “buying” of the business to get started with a new customer. Accepting such a bid carries with it two risks. The first is that the order may go to a less than qualified supplier with the result being bad PCBs. The second is once the link has been established and the customer is dependent on the supplier, prices will escalate beyond what the other bidders quoted.

All of the above discussion seems to imply that the PCB supplier team needs to visit a potential supplier prior to giving it an order. The more complex the PCB is, the more important this survey is.

Along with the need to visit potential PCB suppliers to determine which are capable of building a given PCB, there is the need to real time monitor the deliveries to insure that the quality remains high enough to insure successful manufacture. Due to the fact that personnel change and business models change at fabricators, it is necessary to have periodic re-surveys of existing fabricators. In times of slow down, such as happened in the second half of 2001 fabricator capability can change rapidly, to the extent of some suppliers disappearing altogether, as happened with McCurdy Circuits.

WHAT TO LOOK FOR IN A PCB FABRICATOR

Printed circuit board fabrication is one of the most complex processes involved in the manufacture of electronic products. IC manufacture is perhaps the only manufacturing process that involves more disciplines and more process steps.

PCBs Being Built Just Like Mine

The best and first test of a potential fabricator is to see PCBs of the type being **considered flowing down the production line on a daily basis**. If possible, talk to the customers using those PCBs to see how well they are working out. **Seeing PCBs like yours in the conference room or hanging on the wall does not guarantee the capability of the fabricator**. All too often, the PCBs on display are rejects that have defects that can't be seen visually. Bad PCBs are often displayed in booths at trade shows. At PCB West in the spring of 2002, one vendor had several PCBs on display that were failures from a well-known router vendor.

Sales Engineering Support For Development Engineers

An important component of the fabricator's contribution to a good design is engineering support in the form of advice on materials selection, design rule validation, manufacturability advice and other technical support that is not usually part of the design engineering team's kit of tools. Good support in this area can make the difference between a design that is manufacturable and reliable and one that is not. The more complex the design, the more important this is. The best engineering support comes from fabricators who are routinely building PCBs of the complexity in question. They will have seen many things that can improve the yield of a PCB that a less experienced fabricator has not. **This knowledge is gold.**

Materials Engineering Knowledge

There is a very broad range of potential materials from which PCBs can be built. Most of these materials are good materials. They have been developed to meet a particular need. As an example, paper based materials have been developed to allow very low cost PCBs to be made for simple consumer electronics. Very low loss; low dielectric constant materials have been developed for microwave PCBs. When a material designed for one application is mistakenly used in another, the result is often a failed product.

The more complex a PCB is, the fewer fabricators will have engineers who understand how to select and work with the proper materials. Among the things that must be understood and worked with are how a material shrinks when it goes through the heat of lamination and cool down, how it behaves in the lamination cycle, how it drills, how it plates, how the dielectric constant, ϵ_r , varies across the various thicknesses of laminate and how it varies with frequency. For very high data rate products such as OC-48 and higher, losses in the dielectric, loss tangent, become important as does resistive skin effect losses in the traces.

As controlled impedance becomes more widespread, the engineering team at a fabricator must know how to accurately compute stackups so that impedance of the finished PCB is within limits. This part of the process requires skill in the use of 2D field solvers to accurately calculate impedance and good working knowledge of the dielectric constants of the materials to be used. Fabricators who still rely on equations to calculate impedance will routinely get the impedance wrong, not because of calculation errors, but because the equations themselves are not accurate at the dimensions currently used in PCBs. As a result, equation based impedance calculating methods require trial and error to "tweak" the results in order to arrive at a stack up that yields the right impedance. This is an iterative process that may take multiple fabrication runs. **Using 2D field solvers and accurate materials information results in the right impedance the first time.**

Laminate Materials Types:

A wide variety of dielectric materials are available from which to fabricate PCBs. All are composites of some form of resin system and a reinforcement. They can be divided into two general classes. These are glass reinforced and non-glass reinforced. Woven glass provides dimensional stability to the PCB. All high layer count PCBs must have substantial XY dimensional stability and require woven glass as part of the laminate. (There is one non-glass woven reinforcement that provides this XY stability. It is Gore-Tex® fabric made by W. L. Gore. This material produces a slightly lower dielectric constant composite, but at a very high cost premium. This cost premium does not carry with it a corresponding benefit of equal value.) Other reinforcements include random fibers of Kevlar® and Gore-Tex®.

Virtually all logic PCBs, no matter what the data rate, require glass reinforcement in order to provide the necessary dimensional stability needed by high layer count PCBs.

The following are some examples of glass reinforced laminates.

Low Tg FR-4-	Tg >135C used on thin PCBs, (.062" and thinner)
High Tg FR-4	Tg >170C used on thicker PCBs, (greater than .062")
Getek®	Tg = 185C said to be high performance, but proved difficult to process
Nelco® 4000-13	used on high performance PCBs
Nelco® 4000-13SI	used for low loss PCBs, uses S style glass for low loss
Allied/Isola® FR 408	Getek® equivalent
Allied/Isola® FR 406	Allied version of high Tg FR-4
Nelco 6000-Hi Speed PPE	low loss, but very difficult to process
Isola IS620	used for low loss PCBs, low loss achieved with resin, uses E glass
ZBC®	A Hadco/Zycon® material aimed at creating a large plane capacitor

These are non-glass-reinforced materials.

Rogers RO 4350	used for microwave PCBs
Arlon CLTE	used for microwave PCBs
Teflon based cores	used for microwave PCBs
Speed board	used with other laminated to create selected low loss layers

When multiple types of materials are stocked at a fabricator, there must be some rigorously defined method for insuring that wrong materials are not included in a PCB build. The most common error occurs when a fabricator stocks both low Tg and high Tg materials of the same resin system, such as FR-4. If low Tg material is accidentally used in a PCB that needs high Tg material, the result will PCBs that have failed vias after soldering. This is a disastrous, very expensive mistake, as it results in scrapped assemblies. **Experienced fabricators don't stock low Tg materials for this reason.**

Staff Training

As pointed out earlier, printed circuit board fabrication relies heavily on the skill of the people operating the machinery and maintaining the chemistries involved in the process as well as the skill of the personnel preparing the tooling sets. As with most manufacturing processes, a PCB fabrication process that consistently manufactures high quality PCBs does so only with well-trained and well-motivated people. The more complex the PCB, the more skill is needed for each process. Evidence of ongoing training and certification for each operation should be visible at each station at a good fabricator.

Overall Process Control

PCB fabrication involves more than a hundred process steps. These range from creating photo-tooling, to a variety of chemical cleaning steps, several plating steps, drilling, lamination, testing, coating, materials management and tracking the location of each order in the process. A good fabricator will have the activities involved at each step documented at each station.

Very high on the process control list of important items to monitor is all of the chemistry at every place that a chemistry is used. The best monitoring is real time with automatic systems that have alarms for out of range conditions. Charts should be posted at each step showing how the process is performing on a daily basis with limits shown, so that operators can see how their actions affect the operations.

Chemistries that are not used frequently, such as electroless nickel/immersion gold, can go out of balance to the extent that plating quality is not satisfactory. Therefore, processes such as this that are essential to the successful manufacture of a given PCB must be used and monitored on a regular basis. (This fits into the concept of "PCBs just like mine.")

Front End Processing and Tooling Creation

Front end processing and tooling creation is often referred to as the CAM or computer aided manufacturing part of PCB fabrication. This is where the customer CAD data, fabrication specification and fabrication drawing come together. This activity prepares the job traveler, materials requirements and manufacturing tooling. Manufacturing tooling consists of the photo tools, drilling files, laminate, foil and prepreg kits, lamination schedules, plating schedules, test fixture design files, test files, and silkscreen/legend artwork and instructions.

Data files from customers can arrive by any of several transport methods. A customer can automatically transfer them to a server or it may be requested from a bulletin board at a customer where a designer has posted them. The safest form of transfer is by request from a fabricator after having been notified by manufacturing that the data is ready. Key to the reliability of this operation is very good revision control over all of the data files involved in a design. When revisions must be made after a design has been transferred to a fabricator, it is advisable to roll the revision level of all the files in the data set and send a

completely new set. **Making small changes in a data set already in the hands of a fabricator carries with the risk of inaccurately built PCBs and should be avoided.**

Well-run front-end processes have travelers that are prepared for each type of PCB handled by the shop. There is also a process engineer who examines the design to make sure that it can be built with the data supplied.

Data formats include:

Gerber data in several configurations
RS 274-S
RS 274-X
DXF

Barco DPF
HP-GL
Agilent EEs of Mask
Excellon I & II

Gencam
ODB++

RS-274 X is the most universal. However, many fabricators have used Gerber formats for so long that changing to RS 274 X is difficult. This format has many advantages over of the other formats and should be encouraged.

ODB++ is the output of the Valor CAM system and is favored by many fabricators. The problem with this format is that it is not “universal”.

Design Rule Checking

Design data from a PCB design system consists of data files for each artwork layer, artwork for silkscreens and solder masks, drill data and a fabrication drawing. The first step in the fabrication process is checking that all of the design files are error free, no files are missing and that the appropriate manufacturing tolerances have been included in the design.

A key feature of the DRC operation is the extraction of a net list from the Gerber data that shows how the PCB will be connected if built from the data as received. This net list can then be compared to the net list derived from the schematic- the CAD net list (usually IPC-354 format).

This net list compare must be required for all complex PCBs. A second requirement should be the action taken when there is a disagreement between them. **If a disagreement happens, the job should stop until the disagreement is cleared up.** There is no point in building a known bad PCB.

Other activities involved in design rule checking are verification that clearance specifications are met, that pad diameters are large enough to insure reliable connections, and that all layers register properly to each other.

Panel Sizes

PCBs are manufactured in panels. These panels are usually sized to use the standard sizes of laminate materials. PCB fabricators create special tooling for each panel size they are committed to. It is important to insure that the fabricator candidate has the panel size tooling in place for the PCBs being considered. Failure to do so may result in more expensive PCBs if a larger panel size must be used or delays may result as the fabricator procures the right size tooling and learns how to handle it.

A side consideration when discussing panel sizes is to insure that design engineering knows what the optimum panel sizes are, so that PCB dimensions can be adjusted to make maximum use of the standard panel sizes already in use at a fabricator. The list below has some of the standard panel sizes found in PCB fabricators. The most common is 18” x 24”. The usable area in such a panel is 16” x 22”, so a PCB

of that size would make maximum use of the materials. Moreover, it would insure the widest number of fabricators could be considered as candidates. The bigger the panel size, the fewer fabricators will have tooling.

18" x 24"
24" x 30"

21" x 24"
16" x 18"

24" x 32"

In Asia and Europe there are metric equivalents of these panel sizes that are slightly different in dimensions.

Lamination

Lamination is the process step where all of the layers in a multilayer PCB are "glued" together. There are three components involved in lamination. These are the etched inner layer laminates, the prepreg "glue" layers and sheets of foil that form the outer layers. The glue is normally the uncured resin in the prepreg components of a PCB. There are several methods used in lamination. Some are:

Lamination with heat and pressure only

Lamination with a vacuum bag surrounding the stacked up layers "Turkey bag"

Lamination with the stacked up layers in a press that is inside a full vacuum chamber.

The purpose of the vacuum is to evacuate all of the air from the stack of laminates, foils and prepregs, so no air bubbles are trapped inside after the resins have cured. The more critical the application of the PCB, the more important it is to insure all air is removed. One way to do this without a vacuum is with very high press pressures. High press pressures tend to distort inner layers causing misregistration. **Therefore, the higher the layer count of a PCB, the more important vacuum lamination is.**

A second part of the lamination process is the method used to cool down the PCBs after lamination. The simplest method is to remove the PCBs from the press and let them cool in open air. The problem with this method is the lack of a way to control cool down rate so that the PCB cools uniformly. The result can often be warped PCBs (This is one of the more common reasons for warped PCBs. The alternative to open cool down is to transfer the laminated, hot PCB into a special cool down press, maintain pressure on the PCB and cool it using a gradual lowering of the temperature until room temperature is reached.

There are four types of lamination in use. These are foil lamination, mass lamination, sequential lamination and laminate only lamination.

Foil lamination is the most common method used to produce PCBs of more than two layers. **It is the preferred method for making multilayer PCBs.** It involves etching inner layer pairs back to back on pieces of laminate. There will be one laminate piece for each pair of inner layers. These laminates are then stacked on a plate with pins, which register the layers to each other. The laminates are separated from each other with prepreg, the glue layers, and a piece of copper foil is added to each side.

An alternative to foil lamination using plates with tooling pins for alignment of the inner layers, used in some plants in Europe is to stack all of the inner layers and the prepreg that separates them into a book, secure them together with rivets, add the top and bottom prepregs and foils and then laminate without using alignment pins on the press plates. The argument for using this method for laminating multilayer PCBs is that there is no need for specially tooled press plates, so any size panel can be processed. This is true. However, layer to layer registration is not as precise as when foil lamination is done with tooling pins to align the layers. This is often called mass lamination, but it is not. **It should not be used on high layer count PCBs.**

Mass lamination is a method for laminating four layer PCBs in very large quantities. The inner two layers of the PCB are imaged and etched back to back on a very large piece of laminate, often 36" x 48" or larger. Many PCBs can be imaged on a single piece of laminate. This etched inner layer pair is combined with pieces of prepreg and foil on each side and laminated. After lamination, targets etched on

the inner layers are located in order to line up the drill to each individual inner layer pattern. This local alignment allows very large panel sizes to be used without concern for drill and image tolerance build up across them. This lamination method is used to make very low cost four layer PCBs such as those used for PC motherboards.

Sequential lamination is a method used to build up a PCB when buried vias are required. It can also be used to create blind vias. The layer pair with the buried vias or blind vias in it is drilled, plated and etched using the same process steps involved in making a two sided PCB. This piece of laminate is then combined with the other inner layers, prepreg, foils and laminated using the standard processes.

Cap layer lamination is the original method used to create multilayer PCBs. With this method, the layers are etched in pairs, starting with the outer layers. There is one layer pair set for each two layers in the PCB. Because the outer layers must be solid copper after lamination and drilling to provide a path for plating current, the outer layers are not etched before lamination. The result is a more expensive PCB due to the need to etch one more layer pair than would be required by foil lamination. For this reason, this method is rarely used.

Registration

There are six places in the fabrication process where registration of images to each other is required. These are:

- **Registration of two layers to each other on opposite sides of a piece of laminate.** This is done by the pinning of the artwork to the exposure frame used for “printing” the images on the laminate surfaces. At very well controlled operations, the layer to layer registration accuracy can be within 1 mil.
- **Registration of all the inner layers to each other during lamination.** The most common method for doing this is by stacking all of the inner layer sets on a precisely made plate with alignment pins that mate with precisely punched alignment holes on the inner layer sets. There are two ways to create the alignment holes on the inner layer pieces. One is to punch the alignment holes in the raw laminate prior to exposing the image. This is called “pre-etch punching”. The second is to expose and etch the images on both sides of the laminate. After etching, a special machine picks up targets on the etched image and punches the alignment holes. This is called “post-etch” punching. **Post etch punching is the most accurate of these.** Using this method, layer pair to layer pair registration can be held to an accuracy of 2 mils.
- **Registration of the drill to the inner layer images.** Drilling happens after lamination. The drills need to be aligned as accurately as possible, so that they hit the pads on the inner layers. One method for doing this is to align the drill to the same holes that were used for lamination alignment. Unfortunately, this does not account for any tiny shifts of inner layers during lamination. For best fit on tight tolerance PCBs, targets are etched on all of the inner layers that should fall one on top of the other if the lamination was done perfectly. These targets can be x-rayed after lamination to see how well they are lined up. If there is any misalignment, the x-ray image can be used to fine-tune the drill alignment. **This is the preferred drill alignment process for very high layer count PCBs.**
- **Registration of laser drilled blind vias to inner layer images.** Like through hole drilling, this drilling happens after lamination. Blind vias are used on parts with lead spacing too small to allow through hole drilling. These small holes are often accompanied by smaller than normal pads. These pads are too small to allow for the tolerance build up available to through holes. As a result, there needs to be a method for improving drill accuracy. This can be accomplished by placing laser drill alignment targets on layer 2 near each component pattern requiring blind vias. When this is done, the laser drill first burns away the copper on layer 1 over these targets. This is called “skiving”. The target on layer 2 is used to locally align the laser drill to the pattern on layer 2.

- **Registration of the outer layer images to etch the outer layer features.** The outer layer features that must be lined up with the inner layers are the pads through which the holes have been drilled. This alignment should be done with the same tooling that was used to align the drill.
- **Registration of the solder mask to the outer layer images.** The soldermask must align with the pads that will be used to solder components to the PCB. This alignment should be done to targets that reflect where the pads are. This may not be the same pad set as have the holes drilled in them.
- **Registration of the silk screen or legend images to the outer layer features.** The silk screen and legend artwork needs to be aligned with the component mounting pads. Therefore it should be registered with the same method as the solder mask.

Drilling

Holes in PCBs can be formed in three ways: standard mechanical drilling, laser drilling and chemical etching.

Mechanical drilling is used to create all through holes and can be used to create blind and buried vias. Laser drilling and chemical etching are used to produce blind vias. **Blind vias** are those that start on one side of a PCB, but do not pass all the way through. (By definition, **microvias** are vias with diameters of 8 mils or less. They may be blind or through hole.) **Buried vias** pass between two layers buried inside a PCB.

Aspect ratio, or the ratio of hole diameter to length is a key parameter in the successful plating of through holes and blind vias.

Most good fabricators can properly plate through drilled holes of **aspect ratio 8:1** or less with no special process control in very high quantity. When the aspect ratio exceeds this number, extra care must be taken with hole wall cleaning, maintenance of the chemistry in the plating solutions and the plating currents in order to achieve uniform plating through the entire hole wall of all the holes. At very high aspect ratios, above 10:1, it is likely that reverse pulse plating (PRP) will be required to insure reliable plating.

Plating blind vias that are formed by any of the drilling processes listed above require an aspect ratio of 1:1 or less for reliable plating. In other words, blind vias must not be deeper than they are in diameter. In most cases, it will be necessary to insure that the blind via hole diameter is at least 1.5 times its depth.

An exception to the above restriction on blind vias is blind vias formed by sequential lamination. **Vias formed in this manner are the most expensive and should not be used.**

Blind vias formed by etching is a process that lends itself to PCBs with very large numbers of blind vias. The blind vias are formed using a photosensitive dielectric layer similar to solder mask on the top and bottom of a PCB. This material is exposed to a photo image that allows holes to be etched into the dielectric where vias are needed. Once the blind via holes have been etched down to the underlying layer plating is done as for any other via. This method is most often used when "building up" a PCB layer by layer. **It does not lend itself to large, high layer count PCBs.**

Mechanical drilled hole diameter can range down to as small as 8 mils. As might be expected, the smaller the drilled hole, the more difficult the drilling is and the more expensive the drill bits are. **The smallest drilled hole that can be considered "routine" in PCBs thicker than .032" is 12 mils.** Below that size, extra effort and care must be taken to insure bits are not broken off in a PCB and that the holes are clean after drilling.

Plating Processes and Types

Plating is required on a PCB for two reasons. The first is to form the copper in the drilled holes or vias. This plating makes the connection from one side of the PCB to the other and to the inner layers. The second is to provide a corrosion protection on the copper pads in order to preserve surface in a state that will take solder.

Plating takes two forms, electroless and electrolytic.

Electroless plating is accomplished by using chemistry that precipitates a metal onto the PCB without using an electric current. It is employed two places in the process. These are: to deposit copper in the drilled hole, which is lined with plastic, in order to provide a scaffolding on which to electroplate the hole copper and to deposit one of the surface protecting metals after soldermask has been applied.

Electrolytic plating (electroplating) is used two places as well. These are to plate the copper in the holes to form vias and to plate surface protective metals before outer layer etching and final solder mask is applied.

TYPES OF PLATED METALS

Electroplated copper- Plated on a PCB to form the copper barrels in the vias and other drilled holes. This can be plated with a direct current (the most common) or by a process called reverse pulse plating (PRP). PRP was developed to improve the plating of very small holes (less than 12 mils in diameter) or holes with very high aspect ratios (greater than 10:1). Copper plated using electroplating is more ductile and durable than if plated using the electroless method.

Electroplated Tin/Lead (solder)- This plating is the most common method for providing a protection for the copper in the holes and on the traces as the unwanted copper is etched away to form the outer layers. It can be left on a PCB with solder mask applied over it. If this is done, the plated and etched PCB is usually submerged in a bath of hot oil to fuse the tin and lead into the alloy known as solder. This finish has been all but abandoned because the solder under the solder mask melts during assembly causing shorts.

If the PCB is a backplane, the plated tin/lead can be left on and not reflowed. This provides corrosion protection for the copper in the holes and the tin/lead acts as a lubricant for insertion of press fit connectors. **This is a preferred method for finishing backplanes as it does not subject the PCB to the thermal shock of reflow or HASL.**

Electroplated Tin- Many fabricators are switching from tin/lead as an etch resist to pure tin. This is in response to the drive to eliminate lead from the manufacturing process. This is a good finish for backplanes for the reasons stated for tin/lead. However, if a PCB is to be soldered using reflow or wave soldering, it is possible for the tin under the solder mask to melt causing the mask to flake off. (Solder melts at 185C while pure tin melts at 232C. Good control over soldering temperature can keep this from happening.) **This is also a preferred finish for press fit backplanes.**

Electroplated gold over electroplated nickel- This plating serves two functions. It is used as the etch resist. The gold provides corrosion protection for the soldering surfaces. Nickel is plated on first to provide a barrier between the gold and copper. If this is not done, copper will alloy with the gold and solderability will be lost. **This is the lowest risk surface finish for high density PCBs with fine pitch components.** There is still a risk associated with this finish. The risk is brittle solder joints if excess gold is plated on. The gold plate must be kept at 10 micro- inches or less to avoid this problem.

Electroplated Palladium- This metal is sometimes plated between the nickel and gold in the above finish. It is said to improve the performance of the gold. It is not clear that this helps. It does not degrade the plating of the other metals and should be allowed if a fabricator has it.

Electroless Nickel/Immersion Gold (ENIG)- This finish is applied after the soldermask has been applied over bare copper on the traces. (The solder plated onto the traces and in the holes to provide an etch

resist is removed so it won't reflow under the soldermask.) It provides the corrosion protection benefits of gold. It is electroless because it is applied after etching of the outer layers when there is no path for electroplating. The chemistry involved in this plating method is complex and can go out of balance if not well monitored. The result is a failure mechanism called "black pad". Solder joints fail from this, resulting in unreliable PCBs. **This is not a preferred finish for complex PCBs that must exhibit high, long term reliability.**

Electroless Tin- This finish is pure tin applied as with ENIG and for the same reasons. It does not have the disadvantages of ENIG. It is also cheaper. The problem with it is the tin layer is very thin. When one side of an assembly is reflowed, copper alloys with the tin on the other side making the second solder operation unreliable. **This is a good finish for PCBs with single sided assembly.**

Electroless Silver- This finish is similar to electroless tin. It is said to be less susceptible to second side assembly solder defects. However, there is not enough data collected to substantiate this.

OSP- While this is not a plated finish, it serves the same function- to protect against corrosion prior to soldering. The most common form of this is Entec 106. It is an organic coating that serves as a flux during soldering. The problem this coating has is durability. If it is touched, it fails. If there are two soldering steps, the coating may breakdown enough during the first solder step to cause defects during the second step. **This is a finish that fits low cost, high volume PCBs that are not subjected to handling. It should not be used on complex assemblies.**

Plating Process Controls

Plating is a chemical process. Reliable plating requires real time monitoring of the solutions used in plating. The ideal plating process is automated with computer control of plating currents, plating times and plating chemistry. Hand monitoring and hand plating can result in high quality PCBs. However, this method is dependent on the skill and alertness of each operator. The best plating operation are automated.

Testing

The more complex a PCB, the more likely shorts and opens may occur. To insure that PCBs with these defects don't find their way onto the assembly line, it is necessary to test each one to some standard. There are three possible standards. These are:

The standard may be a learned connectivity based on testing a sampling of PCBs on a bed of nails tester. This is known as "golden board" testing.

Using a CAM station, it is possible to extract a net list from the Gerber data, a Gerber net list.. This list can be used to test bare PCBs. It is more accurate than golden board testing, but still has the potential for shipping defective PCBs if there are errors in the Gerber data.

The connectivity of a PCB is intended to match the net list derived from the schematic. This is known as CAD net list testing. It is the most accurate and should be used as the preferred method.

It is possible to compare the net list from the schematic to that derived from the Gerber data prior to building a PCB. This eliminates the chance that a PCB will be built with a defect that is only discovered after fabrication. **This "net list compare" should be a standard part of tooling a multilayer PCB.**

Test Fixturing

Bare PCBs can be tested with a bed of nails test fixture or with a flying probe tester. Each has advantages. Flying probe testing does not require the creation of a test fixture allowing rapid testing of "quantity of one". However, it is slow and doesn't work for volume manufacture.

Bed of nails testing requires tooling time and cost. It is fast and the preferred method for production test. There are single sided testers and "clam shell" testers for double sided testing.

When surveying potential fabricators it is important to insure testers are available with enough pins and bed sizes large enough to test the PCBs being considered.

SUMMARY

This document paints a rather pessimistic view of the PCB fabrication industry. It makes the industry appear rather undisciplined and lacking in ethics. On the whole, PCB fabricators intend to do the best job they can with the resources at their disposal. Unfortunately, PCB fabrication has been viewed as a somewhat trivial part of electronics by the users of PCBs and good performance has not been well rewarded or recognized. As a result, less capable suppliers have been awarded contracts while the more capable are driven out of business. Sadly, this has been self-defeating on the part of the manufacturers buying the PCBs. This is because the lower bidders deliver inferior products that cause yield problems and, sooner or later, go out of business themselves. After this is discovered, usually at costs far greater than any savings when buying the PCBs, the vendor is disqualified and the search goes on for a replacement.

The process outlined in the above paragraph goes on to such an extent that the capabilities of a fabricator one-year might change dramatically the next. Some may even disappear as happened with McCurdy Circuits in 2001. Some may change their business models completely as Multek did in 2000, going from the best high tech supplier in the world to a mid tier supplier aimed at supplying the needs of the contract manufacturer that purchased it.

It is not the intention to smear the industry, but rather to emphasize the role buyers of PCBs must play in insuring that properly qualified fabricators are chosen for each PCB type and that this supplier base is monitored on a continual basis.

SAMPLE FABRICATOR SURVEY SHEET

CHARACTERISTICS OF FABRICATORS QUALIFIED TO BUILD CUSTOMER PCBs

Customer needs three types of PCBs. These are: daughter PCBs made with Hi Tg FR-4, daughter boards made from Nelco4000-13Si and backplanes made from Nelco 4000-13SI.

VENDOR BEING SURVEYED _____

Requirements for all PCBs.

Data accepted in RS 274-X format _____

PCBs tested to CAD net list _____

Net list extracted from design data and compared to CAD net list prior to build _____

Errors in net list compare resolved in writing prior to PCB build _____

No modifications to Customer A/W without written consent from Customer _____ etch compensation allowed

Lamination done with post etch punch _____

Drill registration done with post lamination x-ray _____

Vacuum lamination _____

Impedance calculation done with 2D field solver, not equations _____

If multiple Tg materials stocked, foolproof method for separating Low Tg from Hi Tg _____

Ability to scale individual A/W layers to compensate for material shrinkage _____

Only glass styles 106, 1080, and 2116 allowed _____

Daughter board requirements- Hi Tg FR-4

PCBs on the manufacturing floor of the complexity Customer is using _____

Panel sizes- 16" x 18" and 18" x 24" _____

Ongoing manufacturing of 24+ layer PCBs _____

Ability to electroplate gold over nickel on entire panel _____

Ability to selectively gold plate 30 micro-inches of gold on BGA mounting sites _____

Ability to drill and plate 13.5 mils holes in 125 mil thick PCBs _____

Impedance testing using traces built into Customer PCBs _____

Measure cross section of finished PCB using stacking stripes provided by Customer _____

Supply at least one photograph with scale of stacking stripes large enough to measure thicknesses_____

Daughter PCB Requirements- Nelco 4000-13SI

PCBs on the manufacturing floor of complexity being considered_____

All of the Hi Tg FR-4 daughter board requirements plus experience with Nelco 4000-13SI_____

Backplane PCB Requirements_

Backplanes on the manufacturing floor of complexity being considered_____

Panel size- 24" x 30" minimum_____

Ability to build backplanes of 36+ layers_____

Drill 26 mil diameter holes through 250 mil thick BP and plate holes to tolerance required by Teradyne VHDM connectors (22 mil +-2 mil finished)_____

All Hi Tg FR-4 daughter board requirements and real time experience with Nelco 4000-13SI

Ability to plate solder on backplane and leave unreflowed (must scrub away slivers)_____

Comments: