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The main scope of this application note is to show the reader how to verify traces on a PCB economically. In today's high speed world, a lot of engineers simulate high speed signals on PC's. This is often done without having a practical feeling for what precisely is happening. Looking at these problems with an 'RF-eye' is something completely different, but a wise thing to do! With this application note I would like to try to give the reader some feeling of RF behaviour into our real analogue hardware world.

This application note will show measurements on 50Ω single-ended and 100Ω differential PCB traces. These differential traces are widely used for CML, pECL and LVDS signaling, backplanes, multiplexers and buses. These are fully differential signal pairs with very low power RF signal levels. They are hard to measure, and it's easy to influence adjacent signal pairs.

Normally, differential measurements are done with 4-port network analyzers, like the Agilent E5071B. These analyzers are not cheap. With this article, I would like to share how we solved this problem by using an affordable 2nd hand HP analyzer, that can be found on ebay today. Included are some good PCB design tips & tricks, especially for high speed design. This article is about PCB high speed design from an RF point-of-view.

If, after reading this article, you have any questions, if you want to discuss matters further, or if you want to share your own experiences in this field, please feel free to contact me at my e-mail address:
pe1rrt at amsat dot org.

Have fun.

ing Marc Simons
August 2003
1. Equipment & Calibration

1.1 Equipment used

This picture shows the HP8753C Network Analyzer (NWA) that has been used for all tests. Although it’s a rather old device, this piece of surplus equipment still is the *de facto standard* for RF network measurements.

![HP8753C Network Analyzer](image)

Most people will probably know the older HP8753A which is the monochrome version. The ‘C’-variant, that I’ve used here, has a colour display. Performance wise there is no great difference between the two. The most important specifications are:

- Frequency range 300kHz to 3GHz
- 50Ω ports
- 110dB Dynamic range
- 3-port measurement: ‘R’ for incident and ‘A’ and ‘B’ for forward & reflected power
- Both Scalar and Vector -measurements
- True S-parameter measurements while using the external S-parameter test set (not yet available for this appnote)

![HP8753C Functional Block Diagram](image)
Later on the HP8753C became the Agilent 8753D with an integrated test set. Today Agilent and Anritsu are the main manufacturers of NWA’s, including multi port versions. Big $$ you need to get one of them, often above $17K We found that most projects economically just won’t cover for the equipment cost alone!

There is an appnote from HP (Agilent) called ‘Network Analysis Basics’ written by David Bello [3]. It’s a set of sheets from their ‘Back To Basics Seminar’. The best you can do is to study this appnote to get more understandings about RF Network Measurements, but if you have dito knowledge, you may proceed or go directly to chapter 2.

**Resistive Power Divider**

Picture 2 (below) is a ‘home brew’ resistive power divider. It has a ripple of +/- 0.5dB from 300kHz..3GHz. Insertion loss is a bit more than 6dB, a typical property of resistive dividers. In practice, the loss is a fraction more due to loss on it’s connectors.

It is easy to make this yourself. Get some scrap GSM base station material, found on HAM fleamarkets (mostly 900MHz). These are stuffed with nicely defined 50Ω striplines on a Teflon PCB. Then, combine SMD resistors to get 3x 16 2/3 W for each leg. What you see in the picture is a part of such a PCB whereon these resistors are fitted to create the divider.

**Dual Direction Coupler**

Picture 3 shows the Agilent HP778D Dual Directional Coupler, which has an outstanding performance in terms of insertion loss and directivity. Coupling 20dB +/- 1.5dB, Frequency range 100MHz .. 2GHz, Primary SWR = 1.1 , Directivity > 30dB. Agilent still has it in production, however, if you find it as surplus it will be more affordable.

A good coupler is not simple to build. There are some HAM articles around showing you how to build one, but then you find that the useful bandwidth is too small and the directivity is poor.

If you have a HP8753D at hand, well, that’s even better. The HP8753D has 2 RF bridges on board. (The same function as the HP85046A S-parameter test set, often found as an addition to the HP8753C). This enables you to do similar measurements as with a HP778D, from virtually DC to 3GHz.
1.2 Instrument Calibration, Verification and Setup

First of all, let us consider about the equipment setup in picture 4. This is the basic setup for most experiments. Basically this is a 50Ω Forward/Reflected power measurement test setup. The Network Analyzer generates a RF signal on the RF OUT source port. The power splitter is giving a portion back to the Incident Input (R) via a 10dB pad. The NWA needs this portion to lock on frequency and phase. The 10dB pad is used to take away 10dB of RF level on the Incident port (R) but also not to feedback port reflections back into the Power Splitter. (Here is why we may use our cheap home brew power divider).

![Diagram of HP8753C setup for forward and reflected power measurements](https://via.placeholder.com/150)

The other half RF OUT part from the Power splitter goes to the 778D Directive Coupler. A 3dB pad prevents strong reflections back to the Power Splitter and so it gives us an extra 6dB mismatch suppression.

The RF signal from the analyzer goes via the Directional Coupler to our D.U.T. the Device Under Test. Reflected power is picked up by the coupler and fed back to port 'A' of the Network Analyzer. Forward power is directly measured on port 'B'. The termination resistor behind the D.U.T. is only used if we want to measure D.U.T's reflection power measurement or just to verify the measurement setup.

Calibration is easy. The HP8753 has a 'normalisation menu' to quickly normalize for cable losses, etc.
2. Unbalanced Measurements

For all measurements we had some boards stuffed with nice traces: The XvampireBoardRev01 reference design from Xilinx. While assembling the first few boards we had an SMD-oven failure. Now these boards became quite handy to do lots of experiments:

2.1 Forward Loss of a $50\Omega$ unbalanced PCB Trace

The easiest measurement was to test one of the $50\Omega$ traces on the XvampireBoard. There are two types of $50\Omega$ traces on the board for doing tests: One on the top layer and one embedded between two GND layers. These traces are 50cm long (about 20 inch) and both are provided with SMA connectors, so this is the easiest test to do with our equipment setup. First the NWA, all cables etc. are normalized to 0dB. In this way we compensate for cable and connector losses. (A good known low loss ‘through’ has been used as D.U.T. !) Then, the PCB was directly connected. See Picture5 on next page for this measurement.

The red line on top is the 0dB reference signal. The vertical scale is 1dB/div. Frequency is measured linear from 300KHz to 1.5GHz. Note the loss: It is 5dB @ 1.5GHz for the embedded trace (green) and 4.5dB for the top trace (yellow). The loss drops nicely linear with frequency. There are no strange things happening, like a complete impedance mismatch, strong impedance discontinuities etc. The main behaviour is linear. Normally you would expect quite a difference in loss from the two PCB tracks. Why is this not the case? The reason for this is the choosen strategy in the PCB layer stackup while designing this board: Never use two GND planes directly around signal layers if they are embedded. The main reason is too much coupling:

$$\frac{1}{\text{Signal\_to\_Ground\_Distance}^2}$$

and hence, counts for both top and bottom side of the PCB trace. This means that the further away the GND layer is, the smaller the coupling to GND will be.

<table>
<thead>
<tr>
<th>Log mag</th>
<th>1dB/div</th>
</tr>
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<tbody>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>4</td>
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</table>

Markers:

1 -2.94 dB  1 GHz  
2 -1.69 dB  500 MHz  
3 -1.07 dB  250 MHz  
4 -3.54 dB  1.25 GHz

Picture 5:
Forward power loss on 50 cm traces on the XvampireBoard
2.2 The OGLP strategy

What is done on the XvampireBoard is that for embedded traces one GND plane is moved a layer more away and it’s original layer is made free of copper. In this way the embedded trace does not have too strong coupling to GND. Only the part where signal traces are placed is made free of copper. The rest still can be used to put GND, to lower the global GND impedance as much as possible. This strategy is called the OGLP strategy: Optimum Ground Layer Positioning. (© YiG Engineering). See also Xilinx UG037 appnote (www.xilinx.com) wherein you can find a good PCB layer stackup and some pictures of the PCB layers, showing this OGLP strategy. (e.g. UG037 is done by YiG Engineering).

There is one very handy and important conclusion we can take here. By using this method it does not matter if the traces are embedded or not. In practice we may also conclude that signal traveling will not vary too much too! This is very nice thing for PCB designers, because now we do not have to bother about length matching any more. The only thing you have to do is using OGLB and to to care of trace impedances (they are different!). Once set, then you’re fine. And please use lots of GND via’s to couple all GND planes.

The OGLB by itself is very easy to setup in your PCB design tool and quite simple to handle! But beware. Again, you still have to consider about impedance matching on each layer and you have to design check your PCB design. You still have 2 GND planes in stead of one, meaning, you have to recalculate your impedance match, and, you have to check if those parts of the GND-planes are really empty. Remember that, because PCB CAD tools do not always allow you to check this in their design rules. Under 2 GHz this method will work very fine. Above 2 GHz, it still will be critical. Your ‘signal propagation’ or ‘signal travelling delay’ on inner layers will be too different from the one on outer layers. So, above 2 GHz it simply is not wise to neglect the difference.

2.3 Return Loss of a 50Ω unbalanced PCB Trace

An interesting thing to do is to have a look on how much of the RF signal is reflected back from the D.U.T. This tells you a lot if the trace you measure behaves as exactly 50Ω and if the trace is properly designed on the PCB.

First, our test setup needs verification. The NWA is going to be used as a reflection test set. Note that quality of cables and connectors is of prime importance! To verify the setup, a dummy D.U.T. will be placed directly on the output of the coupler. First we verify the D.U.T. as an open and then we verify the D.U.T. as an ideal 50Ω termination. Input B on the NWA is not used in this measurement. NWA RF OUT is set to +10dB. Measurements start at 100MHz because of the low frequency limitation of the HP778D directional coupler.

![Diagram of Log mag vs 5dB/div](Picture 6)

**Solid lines**
Directional coupler is left open (green) and shorted with 0Ω (yellow)

Markers:
1 -21.8 dB 250 MHz
2 -19.4 dB 500 MHz
3 -19.2 dB 1 GHz
4 -22.7 dB 1.25 GHz

**Dashed lines**
Coupler directly terminated with a good 50Ω (green) and with a 6dB pad (yellow). These are all reflection measurements.

Markers:
1 -11.0 dB 250 MHz
2 -11.3 dB 500 MHz
3 -12.0 dB 1 GHz
4 -11.3 dB 1.25 GHz
The red line on top is the 0dB reference signal. The vertical scale is 5dB/div. Frequency is measured linear from 100MHz to 1.5GHz in both cases. What you see in these pictures needs some explanation.

The left picture contains 2 measurements: where no load is connected to the Directional Coupler shows you roughly -20dB down. That’s just the coupling factor of the HP778D. With 0Ω directly connected the picture shows you roughly 20dB down too. Note that both measurements will reflect back all energy to the source, hence, giving us a -20dB on the coupler reflected output. All RF is reflected back to the coupler and therefore fed back to the NWA port ‘A’ with 20dB down from the Coupler’s function itself. This strongly verifies our test setup and we may use this level to normalize the NWA to 0dB. In the future we may measure the -20dB on port ‘A’ normalized to 0dB (with respect of the dynamic range of our NWA).

The picture on the right shows you the measurement setup quality: The coupler’s directivity is shown in the green trace after normalisation to 0dB. It’s strange behaviour (extreme directivity peakings etc) is typical for Directional Couplers. The performance of the HP778D shown here is excellent and is > 35dB from 100MHz to 1.5GHz. This means that we can measure reflected signal within a dynamic range of 35dB. To give you a practical feel: 20dB reflected power is only 1:100’s of the original RF signal. If we have this number with our PCB traces, then we would be very happy!

The yellow trace is measured with a 6dB pad mounted as a D.U.T. on the Directional Coupler. The NWA RF is reflected -12dB back into the ‘A’ port. This is what we expect: The signal goes into the 6dB pad, is attenuated 6dB, then it is reflected (end is open!) and attenuated 6dB again. Makes 12dB seen by the NWA. The small ripple is due to the coupling performance and will grow as the D.U.T. becomes exactly 50Ω.

Now we’re ready to do the reflection measurements on the two 50Ω traces: One on the top layer and one embedded with inner layers using the OGLB method. Both traces are 50cm (approx. 20 inch) long:

This behaviour you see here is due to discontinuities of the PCB material composition and thus a discontinuity in it’s εr. Don’t forget: FR4 carrier material is just a bunch of woven glass fibers bond together with some kind of heat resistant resin. Apart from this there is a tolerance in the etching process playing a role here too. Straight PCB tracks are not really that straight. For embedded traces (green) this is even more worse than for traces on top or bottom of the PCB. The worst case reflected shown is -15dB @ 1GHz. This is 1:32 reflection of power from the signal injected in the trace. For 500MHz this is a lot better: -20dB @ 500MHz. This is 1:100 reflection. The impedance of the trace shows impedance between 35 ... 71Ω @ 1GHz and 41 ... 61Ω @ 500MHz. The ripple effect that you see is related to the length of the discontinuous trace. We can make a few practical conclusions now.
2.4 Conclusions, Tips & Tricks

- Design high speed traces only on top and bottom where possible. Geometries in inner layers are smaller thus the tolerances come up stronger! There is also a relation with $\varepsilon_r$. Better having an $\varepsilon_r$ discontinuity on one side of a PCB trace only rather than on two sides!

    **But beware**: Your traces are more susceptible to near field RF energy!

- In practice, with PCB FR4-material, you should expect a maximum return loss of -15dB up to 1GHz. This applies to the given PCB layer stack, 200µ layer thickness to GND plane.

- Not using OGLB would make the embedded results far more worse!

Due to variations in the PCB substrate composition, the $\varepsilon_r$ will vary too. One of the effects caused by this variation is called dispersion. In simple words: Dispersion is a frequency variable delay caused by local changes in the dielectricum $\varepsilon_r$. For a given piece of PCB trace length, the one frequency propagates different from the other. This is a source of phase noise in very high speed designs. Together with attenuation this can break up your design dramatically.

Don’t bother about the effects of dispersion too much. Nowadays lots of people are talking about this subject. It’s all very mind boggling for us: You only have FR4 at your disposal and you need to fix the project, right? Dispersion is only practical to consider above 3GHz. What you see then is that other carrier materials are used, like Teflon®, or even better: ceramics (Rogers®). The best advice I can give you: Design high speed using as much differential signals as you can and use the OGLB method. Single-ended signals travelling over a large PCB will only give you lots of trouble.
3. Balanced Preparations

3.1 The perfect BALUN

Before we can measure traces on a PCB we have to worry about the method we’re going to use. The NWA and all other parts used are all 50Ω unbalanced. For testing PCB traces we need 100Ω balanced. One important thing to create first is a practically ideal BALUN to make the applied RF test signal balanced. Getting from 50Ω to 100Ω is to be taken care of later. (BALUN should be called UNBAL here, but everybody uses the word BALUN for it.)

The best and easiest way to make a BALUN is to put a bunch of ferrite cores over a piece of flex-rigid coax. Do not try to solve this problem with an off the shelf BALUN transformer. This does work well for a small piece of RF spectrum only without too much losses and is very frequency dependent. Also, it will only work under 1GHz. I found 4 assemblies of flex rigid: SMA female connector connected to a 15cm piece of flex-rigid. These were found on a HAM fleamarket for only 2 Euros and were just perfect for this experiment.

The following pictures show how such a broadband BALUN is created:

Picture 8a: Principle schematic of the BALUN

Picture 8b: BALUN made with Ferrite cores on a flex-rigid coax.

Picture 8c: BALUN terminated with two SMD-resistors of 100Ω each (=50Ω).
The ferrite toroids type used here is 3F3 from Ferroxcube. This appeared to be not so critical. Use ferrite cores with a low $\mu$, say, under 100. First, we terminate the BALUN with $2 \times 100 \Omega$ to get a nice $50 \Omega$ terminating resistance. For measuring the BALUN performance the same reflection test setup is used as done in previous $50 \Omega$ trace measurements. Now it is time to check out how good the BALUN works:

For measuring the BALUN performance, the same reflection test setup is used. The yellow curve in picture 9 shows the BALUN terminated, no further connections were made. This behaves like an almost perfectly terminated load as expected. What you actually see here is the quality of the SMA socket, the flex-rigid coax and the accuracy of the $50 \Omega$ termination. The reflected signal is $> 25$ dB down @ 1 GHz, so the power reflected is only $1/316$ of the original RF signal. Now take this: The middle lead(!) of our terminated BALUN now goes directly to GND. The green curve shows the result. Reflected signal is $> 20$ dB down @ 1 GHz, so the reflected power is less than $1/100$ of the original RF signal. Note that all RF-signal is transformed into the shield of the BALUN. Conclusion: It appears to work.
3.2 BALUN-UNBAL Verification

Another way to prove the BALUN’s performance is to connect two BALUN’s together. Solder the middle leads to both and solder the GND’s to both. Then, short the signal lead to GND and do a forward measurement to the NWA input ‘B’. The results are shown in picture10.

First, the NWA is normalized to 0dB with the middle lead floating from GND. Next, the measurement is done with the middle lead connected to GND. By doing this we compensate for the losses of the SMA sockets, the flex-rigid - coax, and the soldered connections. This method is not always preferable. Note the ripple due to discontinuities in the connectors and particularly the soldering link between the two BALUN’s.

As can be seen in the picture, the signal suffers from some loss. Scale is 1dB/Div. Signal loss stays under 2dB @ 1.5GHz. Please note that this measurement is a worst-case performance test. BALUN-UNBAL-BALUN-UNBAL is what’s actually happening here! In practice we don’t need this, but it’s good to realise that it performs so well. Also note that the ferrite doesn’t do anything under a couple of MHz. All signal is lost there. In practice we may conclude that signal loss will certainly stay under 0.5dB for a single UNBAL-action, and 1dB for future measurements: UNBAL to BALUN.

The method used here to design a BALUN is not new. Many manufacturers, such as MiniCircuits and MaCom, use it to create e.g. 4-way broadband power splitters. If you can find one of these as a surplus part, do not hesitate and buy it! It often contains the best ferrites available for creating a good BALUN, performing upto 2GHz. For those interested in BALUN’s and ferrites, I’d like to recommend Rothammels Antennenbuch. Although it’s written in German, it contains many nice experiments and examples on the subject.
3.3 Going from 50Ω to 100Ω Impedance

Now it is time to consider how to convert from 50Ω to 100Ω and back. Some experiments were carried out with 1:2 impedance transformers. This worked up to 1GHz. However, the initial return loss was so bad, that it was impossible to verify what we were measuring; the transformer or the PCB trace? Not to mention the variation in transformation over frequency of these transformers.

Therefore, the only good solution at hand was to design a passive Impedance Matching Pad. It’s relatively simple and it has a wide bandwidth. The only disadvantage is its loss. Once connected to the BALUN we’re able to carry out measurements on a 100Ω balanced PCB pair. The best method to verify such a Matching PAD, is to use the NWA setup, just as before.

At this point I would like to draw your attention to an EDN-article written by Howard Johnson PhD called Matching Pads [7]. Creating the Matching PAD is not difficult. Here are a couple of formulae which can be used to calculate PAD resistors.

\[
R_2 = \frac{Z_1 \cdot k}{k} \quad R_1 = \frac{Z_2}{k} \quad k = \sqrt{1 - \frac{Z_1}{Z_2}} \quad G_{12} = (1 + k)^{-1} \quad G_{21} = 1 - k
\]

Let us consider the transformation from 50Ω to 100Ω. We have: \(Z_1 = 50\,\Omega, Z_2 = 100\,\Omega\Rightarrow k = \frac{1}{2}\sqrt{2}\)

Picture 11: PAD Resistor calculations for impedance matching purposes

(Please note that one of the formulae in the original EDN-article contains a misprint)

Calculating the two resistors \(R_1\) and \(R_2\) will result in a value of 70.7Ω each. Calculating the gain \(G_{12}\) from 50Ω to 100Ω will result in 0.586. Calculating \(G_{21}\), to go back from 100Ω to 50Ω, will result in 0.293. Let us consider the insertion loss when these two are connected.

The loss over the 2 PADs is \(G_{12} \cdot G_{21} = 0.1715\). The PADs insertion loss = \(20\log(G_{12} \cdot G_{21}) = -15.3\,\text{dB}\). When compared with a table for resistive PI-networks (for example the ARRL Handbook), you’ll find a comparable loss, which proves that our calculations are correct.

We may now split resistor \(R_2\) into two equal parts. This way, our circuit becomes symmetrical which is exactly what we need for a balanced system. Next, we need to build the required resistor values from components available in the E24 series.

Picture 12: PAD Resistors transferred to balanced + practical values with their tolerances
Using the NWA Transmission/Reflection test setup we will now measure the reflection and insertion loss for the impedance matching circuit. For reflection we found the following results:

A single Matching Pad is terminated with $100\Omega$. Ideally it should now behave like a regular $50\Omega$ terminator. However, due to the PAD construction, it never will be as good as a high quality $50\Omega$ SMA terminator. Frequency range measured here is 300KHz.. 3GHz. Vertical scale is 5dB/Div. The green curve is the $50\Omega$ SMA terminator, the yellow curve is our terminated PAD. The results are satisfactory: Reflected power is $< 23$dB to 3GHz! A few intermediate conclusions can be given:

- PAD construction is crucial here! Care should be taken to keep distances ultra short and to use SMD resistors shape 0603. The shorter the distances, the less the reflected power will be

- As shown, the HP778D coupler in use performs well, even above 2GHz. The directivity only drops by 5dB. (The HP778D is specified to 2GHz, but we use it to 3GHz in our measurements.)

- In general we’ve lost about 5dB of directivity due to the quality of the cables and connectors used.
Connecting 2 matching PADs together, will form a resistive Pi-network attenuator. We will now try to measure the insertion loss. Based on our previous calculations it should be 15.3 dB.

| Markers: |
|-----------------|-----------------|
| 1 | -15.4 dB | 500 MHz |
| 2 | -15.7 dB | 1 GHz |
| 3 | -16.3 dB | 2 GHz |
| 4 | -16.9 dB | 3 GHz |

Start: 100 MHz  Stop: 3000 MHz

The picture shows a spectrum from 100MHz to 3GHz. Vertical scale is 2dB/div. The combined insertion loss for the 2 Pad's is quite constant and is about 15 .. 17dB. What is shown here too, are the two PAD terminals connected straight (blue curve) and twisted (red curve) to take the BALUN’s performance into account as well.

Close to 100MHz, the loss is 15.3 dB, which is exactly as expected. Going up in frequency, will show a higher loss. This loss is caused by the discontinuities of the SMA connectors and the resistor PAD itself. Of course, the latter dominates. These results are good enough to measure 100Ω differential PCB traces in our real world. Maximum PAD loss is < 1.5dB for frequencies between 100MHz and 1.5GHz.

Picture 14a:
Insertion loss with 2 100Ω Impedance Matching PADs are connected.

Picture 14b:
View on the physical Matching Pads connected together. It forms a discontinuity. Lots of hotmelt was used here to keep it all together.
3.4 Defining the individual PAD reflection at unmatched impedance

As shown previously, we found that the PAD’s reflected power is rather low. Terminated with 100Ω, it acts like a 50Ω termination with some discontinuity, resulting in a small mismatch from 2GHz onwards. The final issue to be solved here is to have a look on reflected power if a individual PAD is not terminated with 100Ω. With its terminals shorted, the PAD becomes part of a badly terminated transmission line. The effective termination resistance will be 35.35Ω (70.7Ω // (35.35Ω + 35.35Ω)).

For this reason we may expect some reflected power. Please note that this situation will generate the highest possible reflection for this BALUN + PAD combination. (From now we will call this combination just PAD)

If the PAD is correctly layed out and soldered, the reflection should be constant over the full frequency range. The following picture shows the reflected power of the shortened PAD (yellow curve) compared to that of a good 7dB attenuator (green curve). NWA is normalized to 0dB leaving the Directional Coupler open or shortened, exactly as we did in previous measurements.

This result is not too bad: upto 2GHz the two curves are in the same order of magnitude. The ripple you see is caused by the Directional Coupler’s wideband directional behaviour.

We may now draw the following conclusions:

- BALUN performance is perfectly okay. A pair of PAD’s will give a balancing error of only 1dB.
- Resistive matching from 50Ω to 100Ω and back from 100Ω to 50Ω will give a loss of approx. 15dB.
- The PAD can be used to measure the reflection on a 100Ω balanced PCB pair.
- The maximum reflection range we can measure is 15dB. This is caused by the 70.7Ω resistor in the PAD.
- The PAD is good enough for through- and reflection measurements up to 2GHz.
4. Balanced Measurements

4.1 Signal Path Loss

Using the NWA setup from picture4 and using the two PAD’s, the loss of 100Ω PCB signal pairs can now be measured. First, we ground our test PCB to the NWA GND with a very short thick litze-wire (>2cm thick). The D.U.T. is the 2 PAD’s combined with the PCB pair. First the NWA must be normalized to 0dB with the 2 PAD’s connected together. To give you an idea: All cable influences, frequency dependant loss of the PAD’s, etc. will be normalized to 0dB. This is done to isolate their loss so we can see what the PCB signal pair does on it’s own. Then, the 2 PADS carefully must be soldered to the balanced pair on the PCB board. Wiring to the PCB is only one mm long! Picture 16 show you the PCB pair losses:

Log mag 1dB/div

Start: 100 MHz
Stop: 3000 MHz

Markers:
1 - 2.3 dB 500 MHz
2 - 3.5 dB 1 GHz
3 - 5.4 dB 2 GHz
4 - 8.0 dB 3 GHz

Picture 16a:
50cm long 100Ω PCB pair losses on top layer from 100MHz to 3GHz

Picture 16b:
PCB board measurement with the 2 Impedance Matching PAD’s shown
The same measurement method for a pair of 100Ω embedded traces. These are also 50cm long.

![Graph showing measurement data with markers and frequency range from 100 MHz to 3 GHz]

Markers:

1. -2.9 dB  at 500 MHz
2. -4.0 dB  at 1 GHz
3. -5.2 dB  at 2 GHz
4. -8.4 dB  at 3 GHz

These measurements show about 1.5 dB difference in loss between picture 16, the top layer PCB pair and picture 17 the inner layer pair. As proven with the 50Ω tracks this small difference is due to the OGLB method. Again, not using this method would result in a dramatic difference between the two! To match trace length on its own is hard enough during the layout session of your board. Herewith we proved that with only 1 dB for half a meter we are perfectly fine.

Frequency range in these pictures is from 100 MHz to 3 GHz(!). Vertical is 1 dB/Div. The difference between the red and the blue line shown is where we have twisted one of the PAD’s leads to the PCB. It again shows you that the two BALUN’s do their job fine. These measurements can be used as a practical reference too. The actual signal losses will stay in between the red and blue curves. In our CAD-station, the PCB pairs setup was:

- On the top layer trace width = 7.0 mil, spacing 5.5 mil. Layer thickness to GND = 200 µ
- On the inner layers trace width = 5.0 mil, spacing 6.5 mil. Layer thickness to GND = 200 µ on one side and 435 µ on the other side. (i.e. OGLB method is used).
- Copper thickness = 35 µ

As a rule of thumb in digital transmission the bandwidth of the medium needs to be at least 0.8 times its bit rate. At 800 MBit/Sec we need 0.8 • 800 MBit/Sec = 640 MHz. The attenuation at this frequency can be read from the measurement and is 3 dB. The nice thing about these results is that you can get a good practical feel how much loss a 100Ω pair will give you over a certain distance and frequency. The measurements shows you that this relation is rather linear.
4.2 Balanced PCB pair reflection

Final thing to do now is to have a look on the PCB pair power reflection. Following strategy is used:

- Setup the NWA for reflection measurements
- Terminate the Impedance Matching PAD with a short
- Measure the reflected power from the PAD and normalize this to 0dB
- Put 100Ω on the PAD and measure it. This is stored in NWA memory (green) as 'best absorption to expect'
- The reference base (red on top) is the worst reflected power
- The PCB pair must be terminated at its far end with 100Ω
- Now measure the actual PCB pair
- Compare the results we got, see next picture

![Log mag 5dB/div](image)

Markers:

1. -28.5 dB, 500 MHz
2. -15.6 dB, 1 GHz
3. -14.3 dB, 2 GHz
4. -10.5 dB, 3 GHz

Picture 18:

50cm long 100Ω PCB pair on top layer reflected from 100MHz to 3GHz

Most relevant is to notice the difference in the yellow and the green curve. The closer they are, the better the PCB pair behaves like a perfect 100Ω impedance. The yellow trace is the reflected power from the measured PCB trace, terminated at the far end with 100Ω.

As you can see the PCB pair with the termination resistor absorbs almost all power nicely to 1.5GHz. Then some more power starts to reflect. However, it is not bad because it is an extra 10dB absorption on top of what the 70.7Ω in the PAD already does for us. From 1.7GHz and further on the PCB starts to reflect more power back to our PAD. At 2.5GHz you can even see that it reflects back all it’s power. The measurement has become unusable here.
The measurements in picture19 are done on the embedded signal pair. Note that these have a very close relation to the previous measurement. This is due to the OGLB-strategy.

Due to losses in the PAD's our reflected measurements done here are a bit 'so so'. Not too much headroom because of the 15dB we only have due to the matching PAD. We have to find another solution for that. Doing 'through' measurements was going perfectly okay. With a dynamic range of the NWA of about 110dB we still had more than enough headroom.
4.3 Final Conclusions & Advising Notes

- There is one very handy and important conclusion we can draw here: By using OGLB it doesn’t matter too much whether the PCB signal pairs are embedded or not. Our measurements here proved this. In practice we may also conclude that signal travelling speed will not vary too much either! This is very useful for PCB designs. Matching trace lengths will be much easier: both top and embedded layers can be treated identically. As long as the frequency stays under 2GHz, we are fine. However, you still have to take controlled impedance into account.

- The above conclusion is not a green light just to place these balanced pairs everywhere you want though. Lots of mistakes can still be made. Always be aware of what you do. Have a good reason for every via-pair you put in the signal path, as via’s form discontinuities and stubs! Try to find some good PCB layout application notes on the web if you’re in doubt. Read your articles carefully. The web is full of bad designs, but there are some good examples as well. National Semiconductors is one of the leading companies with good LVDS application notes. Fortunately, these guys always have been very aware of analogue design.

- Do not try to put more than 1.5GHz – 2GHz on 100Ω differential FR4 PCB pairs over long distances. This is due to discontinuities in \( \varepsilon_r \) (the FR4 dielectricum) and due to PCB etching process tolerances. If you want to go faster, you'll have to move to the top or bottom layer only, or you have to choose another PCB substrate. Rogers® 4350 is a good example.

- On the web you often see articles where TDR equipment is used to measure PCB tracks. (TDR = Time Domain Reflectometry). It is used to measure the characteristic impedance of transmission lines, backplanes and their connectors. What you don’t see is the mistakes people make with TDRs. I’ve had a situation where beautiful measurements were made with a very bad patch cable between the TDR and the D.U.T. The results were in no relation to the D.U.T. to be measured. You have to validate and verify your measurements and methods, again and again, just as shown in this article.

- The measurements as described in this article have some amazing and maybe unexpected RF behaviour. Without a good field solving simulation tool you simply cannot beat measuring the real world. (Except when things physically become too small to measure). Spice won’t do here any good. Signal behaviour on PCB is too complex. for IBIS this is even worse. The models used are often just too simple.

- Please don’t believe in board simulation tools. If you have an RF problem, consider it as a local problem to solve. Split your problem up. How do I go to another layer without too much loss? How far away do I need to layout my pairs, so they do not couple too much? How do I get my LVDS pairs out of my FPGA? In some way these questions can all be seen as local problems. If you critically look at board simulation tools, you'll see that in most cases they've used simple Spice models for each of the problems on the board. In that approach, a number of significant parameters are not taken in to account. You might be better off buying some good pieces of surplus measurement hardware, instead of paying big $$$ for annoying software you never will use anyway. And don’t forget: if you use simulation tools, most software houses will charge you for 20% of those big $$$ each year, again and again! And don’t forget about your time too.

- If 95% of your time is occupied with creating VHDL designs and your boss asks you to design the high speed PCB as well, then simply DON'T! You have to spend lots of time before you’ve acquired the analogue & RF awareness to be able to design such boards.

- RF engineers are always willing to explain things to you. Others may only spread misty theories. Luckily they often are radio amateurs (HAM’s). Between HAM’s there is a spirit to share knowledge. Make use of that and don’t forget to share your knowledge with them too! (It is called: HAM-spirit.)

- If you would like to share something related to RF & PCB board design? Please do so! Mail to: PE1RRT at Amsat dot org. My name is Marc Simons.

~fin~
Appendix A

Used Literature

1. **UG037 (V0.4) July 24, 2003 Appnote Xilinx XlvdsPro Demonstration Boards**
   Marc Defossez, Xilinx Inc.
   page 37: Fig 1-14: PCB Layer Stackup, and next pages for having a look on the PCB layout + methods.

2. **The ARRL (Americal Radio Relay League) handbook 1999**
   Page 30.24: Pi resistive Attenuators
   Page 30.25: SWR and return loss equivalents table

3. **HP (Agilent) 'Network Analysis Basics'**
   David Bello
   Set of sheets & text from their Back To Basics Seminar on Network Analyzers.

4. **RF Circuit Design -- Theory and Applications**
   Reinhold Ludwig & Pavel Bretchko, Prentice Hall
   Page 92: Return loss of transmission line section

5. **Agilent Appnote 1291-1B: '10 Hints for Making Better Network Analyzer Measurements'**

6. **Rothammels AntennenBuch (12. aktualisierte Auflage)**
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   Page 143: 7 Symmetrie- und Sperrglieder
   Page 159: Transformationen mit W2DU-Baluns
   ISBN 3-88692-033-X

7. **Matching Pads (article)**
   Howard Johnson PhD
   EDN December 2001 (www.ednmag.com) (Google: Matching PAD EDN)