TEST LAB ARTICLE FOR PCB DESIGN MAGAZINE.

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This article is the second in a continuing series of articles intended to examine the large collection of rules of thumb that circulate in the PCB design and EMI engineering communities.

This article examines two more rules of thumb: Cuts in power planes cause signal integrity problems; and solder mask alters the impedance of traces running on surface layers. The effects of vias on signals will be covered in the next installment.

The test vehicle for this series of experiments is a 14 layer 7” x 10” PCB especially designed to allow measurement of these effects as well as other phenomena. Figure 1 is a copy of the layer 1 artwork showing arrays of vias aimed at quantifying the effects of vias as well as an array of traces aimed at measuring cross talk, effects of right angle bends, presence of solder mask and trace width vs. impedance.

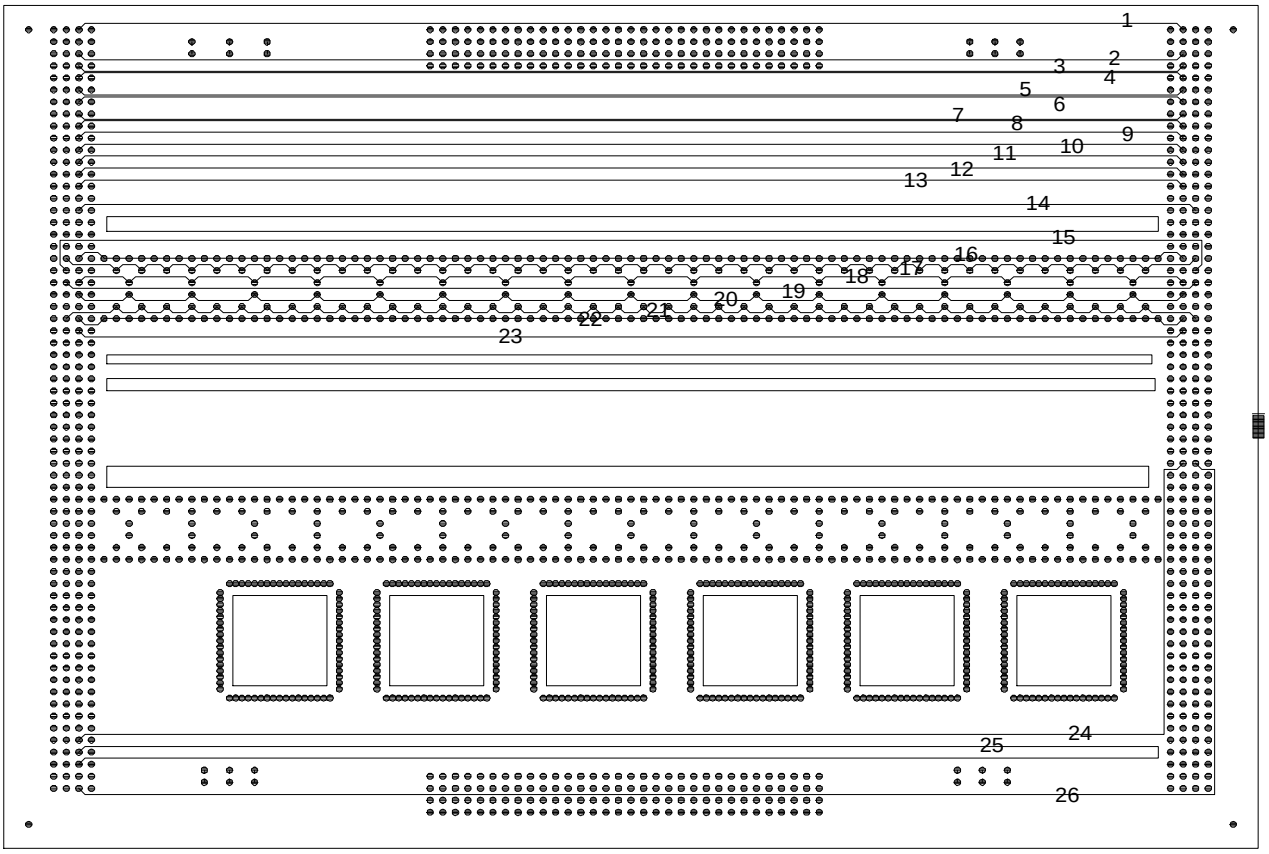

Figure 1; Layer 1 artwork for test PCB.

Figure 2 shows the cross section of the test PCB. It is a 14 layer PCB with a wide variety of dielectric thicknesses and transmission line types to provide the broadest selection of test structures. This test PCB is often used to validate the results of various simulations by measuring actual signal behavior in the test PCB and comparing it to the simulation results.
The desired dielectric thicknesses are shown inside the cross section. Actual dimensions in the finished PCB are shown at the right.

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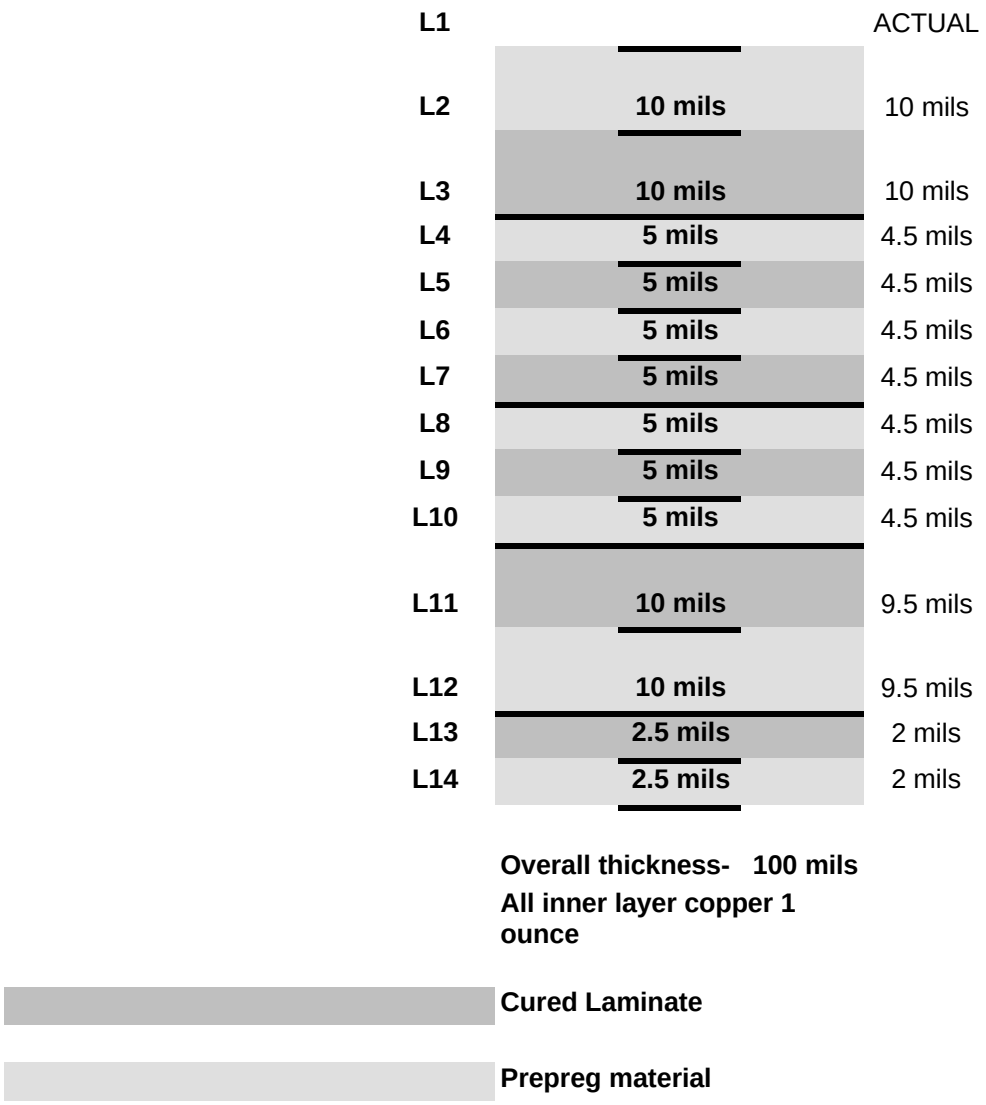

TEST PCB CROSS SECTION

Figure 2, Cross-section of Test PCB

TRACES CROSSING PLANE CUTS.

Traces 1 through 14 shown in Figure 1 all cross a 10 mil wide plane cut in the power plane immediately underlying them. This plane is layer 3, approximately 21 mils below the trace layer. Figure 3 is a TDR scan of the impedance of trace 3. The TDR edge rate was 125 pSec. The plane cut is approximately 2/3 of the way from the left end. As can be seen from the scan, there is no reflection of any kind where the trace passes over the plane cut. This signifies that there is no detectable change in impedance at the cut. When one moves a near field probe over this trace, no emissions are detected as well. Why is this?

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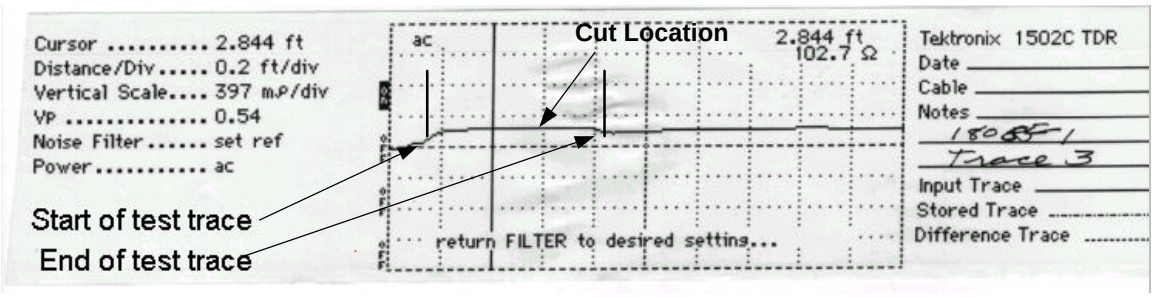


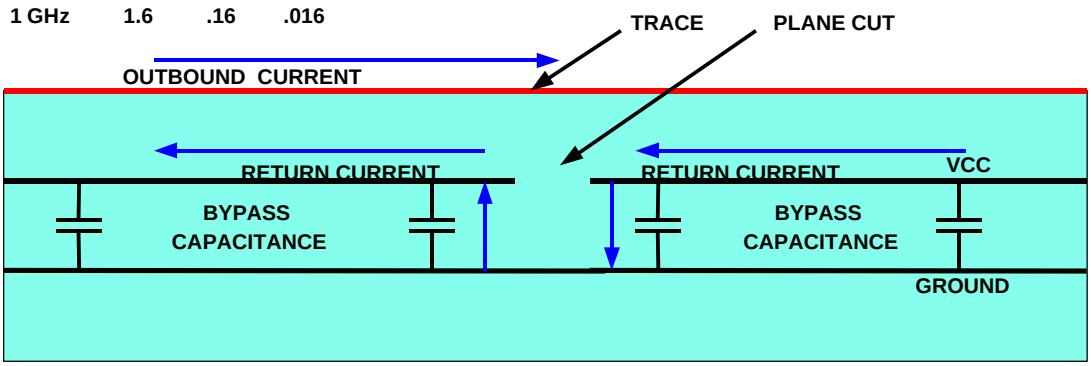
Figure 3, TDR Scan of trace number 3 passing over a cut in underlying power plane

The electromagnetic field that propagates along the trace creates an outbound current on the trace and a "return current" on the underlying plane. When the plane is cut, it might be expected that the return current will have to travel out around the cut creating a large current loop with a resulting high EMI field and possibly some disruption of the signal itself. This does not happen. Figure 4 shows how the currents flow around cuts in planes. As long as there is a second plane underlying the plane with the cut and there is sufficient capacitance between the planes, the return current will flow under the trace through this capacitance.

Howard Johnson demonstrated this with an experiment involving a wire passing over a slot in its underlying plane. He then "stitched" the two sides of the slot to a second underlying plane that was continuous, using bypass capacitors. After the "stitching" the emissions went away.

CAPACITIVE REACTANCES vs. FREQUENCY

FREQ	100pF	1000 pF	.01
30 MHz	53	5.3	.53
100 MHz	16	1.6	.16
1 GHz	1.6	.16	.016



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PATH OF RETURN CURRENT WHEN SIGNAL LINE CROSSES A PLANE CUT

NOTE: BYPASS CAPACITANCE IS MADE UP OF DISCRETE CAPACITORS AND INTERPLANE CAPACITANCE. FOR FAST EDGES, THE INTERPLANE CAPACITOR DOMINATES.

DC NAMES OF PLANES ARE UNIMPORTANT, SO LONG AS BYPASSING IS PROPERLY DONE.

Figure 4, Path of Return Currents Around a Plane Cut

What these measurements illustrate is that plane cuts will not adversely affect high speed signals that cross them so long as there is a second plane that is tightly coupled with bypass capacitors and interplane capacitance. This capacitance provides an AC path for the currents associated with the signal. Note: In the process of providing bypass capacitance of sufficient quantity and

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quality to support the switching edges, the capacitance necessary for signals crossing plane cuts will always be there. This fails to be true if the plane cut occurs in both or all planes in the same place.

The table in Figure 4 shows capacitive reactance vs. frequency for three common values of bypass capacitors. From this, it can be seen that good power supply bypassing will provide the current paths needed across splits in planes.

SOLDER MASK CHANGES TRACE IMPEDANCE ON SURFACE LAYERS

There is often concern that solder mask will alter the impedance of traces on outer layers and that this change may be significant. Trace 24 is a 5 mil trace on layer 1 covered with solder mask. Trace 25 is another 5 mil trace on layer 1 without solder mask. Figure 5 is a TDR scan of

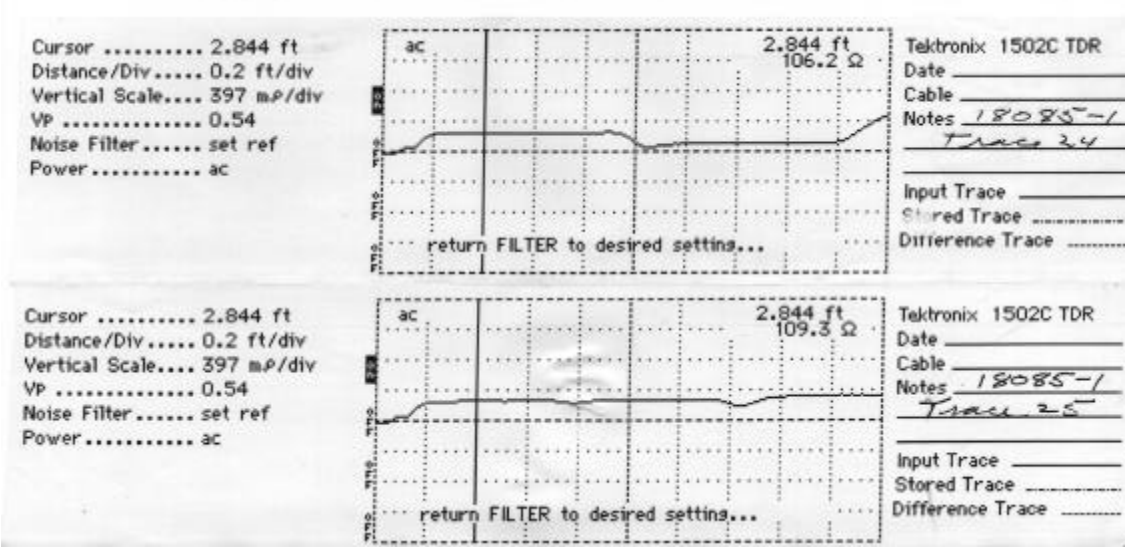

Figure 5, TDR Scans of 5 mil Wide Surface Traces, Top Covered With Solder Mask, Bottom, no Solder Mask

the two surface traces, trace 24 on the top and trace 25 on the bottom. The solder mask is a liquid photoimagable material with a thickness of 0.5 mils or 200 microns. From this test it is clear that adding solder mask lowers the impedance of traces on surface layers.

None of the standard impedance predicting equations allow for this effect. As a result, surface layer traces covered with solder mask always measure lower than predicted. How does one compensate for this? There are no reliable equations one can use. However, there is a way to solve this problem. The method is a 2D or two dimensional field solver. When the dimensions measured for the structures represented by traces 24 and 25 are entered into one of the popular 2D field solvers, the calculated impedances are 106.5 and 109 ohms, respectively.

Note that the electrical length of trace 25 is twice that of trace 24. From Figure 1, it can be seen that trace 25 goes out and back in a U shape. There is an impedance dip in the middle of trace 25. This impedance dip is caused by a large amount of solder deposited on the connecting link at the right end of trace 25.

Summary

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Rules of thumb often have sound foundations in their original presentation. However, when taken out of context, as is the case with the split plane rules of thumb in common circulation, they often result in design rules or constraints that add cost without benefit. Even worse, they often cause a designer to think that high-speed problems are under control when they are not. In the case of the various split plane rules, the important issue that is not dealt with is good power subsystem design which includes proper use of bypass capacitors and plane capacitance to create a robust power subsystem.

The reader is advised to view all rules of thumb with a certain amount of scepticism and insist that the proposer of such rules provide the science that supports such rules. Failure to do so often results in designs that costs more than it should and still doesn't function properly.

References:

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