

SIMULATION AND ANALYSIS

A beginners guide to what they are and why they are needed.

By Lee W. Ritchey, Speeding Edge, Copyright, June 1998

Introduction

As products become more complex, the speeds of logic devices continue to increase, the pressure to get products to market in shorter time spans increases and the need for a development process that insures proper function over the extremes of operational environment and component tolerances steadily rises. As a result of these conditions, talk in the design group begins to center on simulation and analysis as a necessary part of the process. In fact, some would say that the first competitor to successfully exploit these methods would win the day and that often turns out to be the case. Some like to call these design methods electronic or virtual bread boarding.

Although Simulation and Analysis as concepts have been in use for many years, they are new to many engineers and designers who must find a way to “get up to speed” or risk being left out of the development process. This article explores what simulation and analysis mean, how they help the development process, how to implement them and what the consequences are.

The Design Objective

The end objective of the development process is to launch onto the production line and into the market, a product that is cost effective, manufacturable, reliable, on time and unconditionally stable. The first four of these objectives are relatively clear to most of us. The fourth, developing a product that is unconditionally stable, needs some clarification.

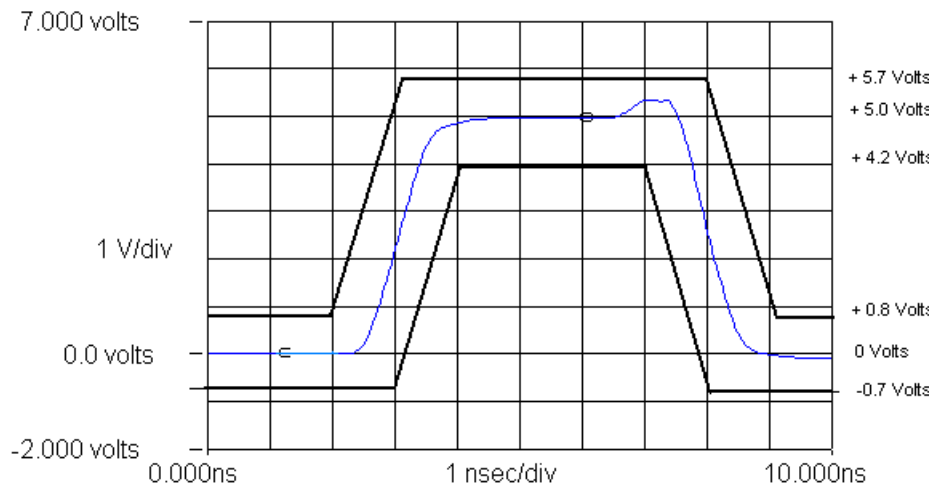


Figure 1 A Typical Logic Signal Showing the Envelope of Allowed Values

Figure 1 shows a logic signal with the envelope of allowed values surrounding it. This envelope is defined by the maximum and minimum input voltages required for a logic device to operate properly and by the timing tolerances in the system timing budget. For a system to be unconditionally stable, all of the sources of error in a system, when added together must not cause the signal to extend outside this envelope. Using bread boarding and prototyping techniques can't provide the assurance that a design will meet these conditions for all possible combinations of part speeds, gains and packages that will be used.

Variables That Affect Design Stability

Design stability can be affected by timing errors as well as voltage levels that stray out of bounds.

The elements that can cause timing errors include:

- Length of routed traces in the PCB
- Differences in length of routed traces within a single bus or logic path
- The propagation delays of the ICs in the design
- Variations in propagation delays of the ICs used in the design
- Loading along the length of a net

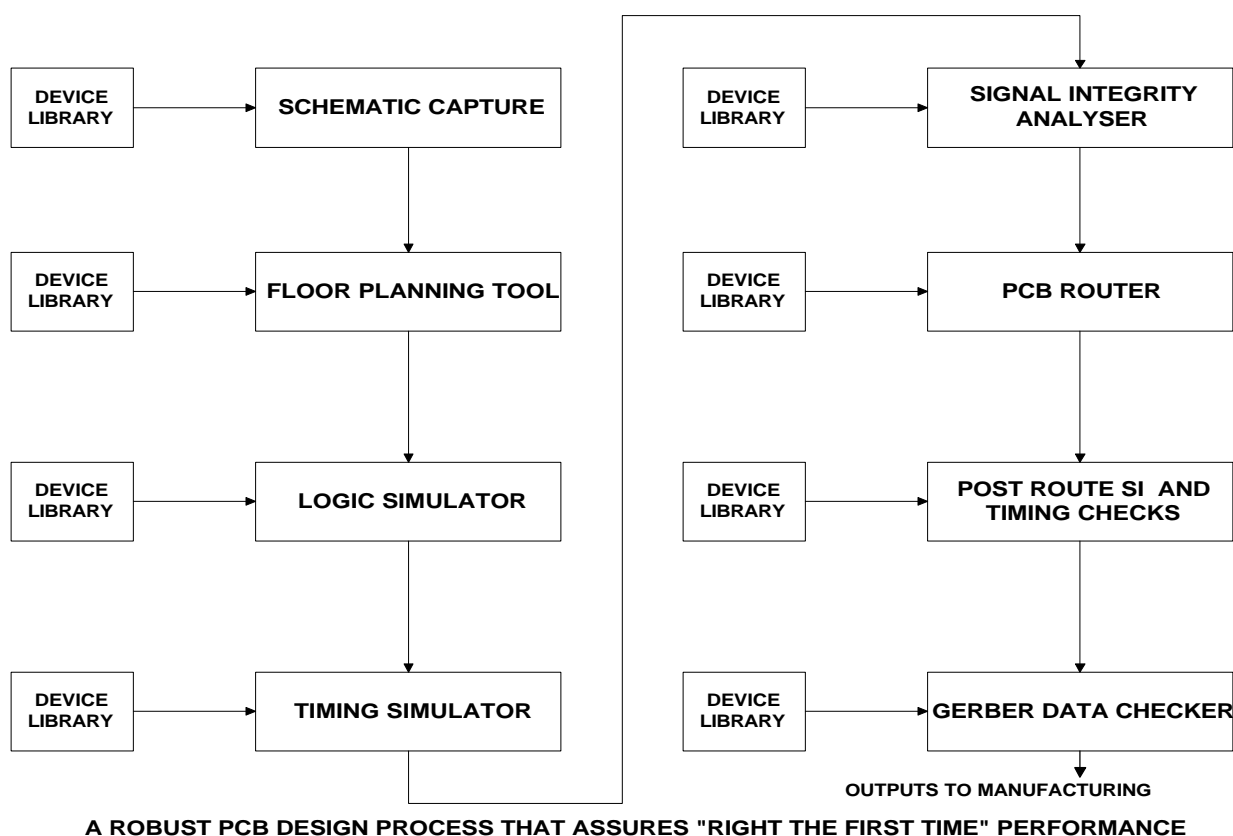
Those variables that can cause the voltage levels to stray out of bounds include:

- Reflections from trace discontinuities
- Lack of terminations on transmission lines
- Poorly matched terminations on transmission lines
- Coupling from adjacent signals
- Ground or Vcc bounce caused by package lead inductances
- Power supply variations
- Temperature variations
- Noise on power supply rails
- Variations in output voltages due to loading
- Connector discontinuities

From the foregoing, it is easy to see that there are too many variables to account for all of them with a prototype or a pilot run. Fortunately, the tools and methods needed to properly analyze the effects of each of these variables are reliable and readily available.

A Design Process To Validate Product Stability

Figure 2 depicts a PCB design process intended to account for all of the aforementioned variables. An obvious difference of this design process from most others is the “continuous” flow of the design from step to step. Also missing is the division between the engineer and the PCB designer. A successful design process is dependent upon on merging the activities of these two disciplines so that there is an overlap of one skill set into the other. This does not mean that the PCB designer gets removed from the process. Instead, the skills and knowledge that a PCB designer possesses relative to how best to do routing; how to create tolerances for the features in an artwork for optimum manufacturing yield; and how to create the documents and files required to fabricate, assemble and test a PCB are more important than ever. Further, in order to properly participate in this process, the PCB designer must understand it and his or her role relative to it.



PREPARED BY LEE RITCHEY 12/2/97

Figure 2 A Design Process With Full Simulation Processes

Several blocks in the design process look familiar to most of us. Among these are schematic capture, PCB routing and Gerber data checking. These are the traditional steps in the PCB design process. The remaining blocks are part of the “right the first time” design process and are likely to be unfamiliar to most designers. We will examine them one at a time.

Floor Planning Tool

The floor planning tool is tightly coupled to the schematic capture tool on the design engineer's desk. This tool allows the design engineer to place the components of a design on a virtual PCB and explore the effects of component placement on thermal profiles, net lengths, routability and signal quality. This is a "what if" tool that makes it possible to perform tradeoffs among the many conflicting requirements a design must meet without needing to do actual PCB layout. The output from this tool is a trial placement, instructions to the router on length of signal paths, ordering of points in nets, values and locations of terminations and other constraints.

Logic Simulator

Logic simulators are employed to create virtual logic models of designs in order to verify that the logic design performs the desired function without the need to build real hardware. These tools have been the backbone of the semiconductor design industry for many years. Without them, it would be necessary to make several passes through the routing, fabrication and test process before arriving at a solid design. These same tools are available to those designing PCBs and systems. Logic simulators are software tools that create a logic model of a design in software and then run this model at the speeds at which the computer can operate. For complex designs, the simulation speed may be so slow that full simulation is not practical. To solve this problem, hardware emulators have been designed.

Hardware Emulators are made from programmable logic devices that allow the designer to create a hardware model of a design. These hardware models are capable of running simulations at many orders of magnitude faster than the software-based models. In fact, these hardware emulators are often used to run the actual final software prior to building any hardware at all. In many cases, it is possible to run all of the operating software on the hardware emulator in such a way that the emulator can perform all of the functions of the final hardware. This is precisely the method used by Intel to design its Pentium IC set.

Timing Simulator

A timing simulator does the task that its name implies. It is a software model of all the signal paths through a design with delay times for the silicon and wire included. Maximum and minimum time delays through each semiconductor are loaded into the models. During the simulation process, the delay through each path is varied between maximum and minimum, much like would occur in real hardware, to verify that the timing budget has made allowance for the normal variations in production parts.

Signal Integrity Analyzer

Signal Integrity Analysis (SIA) is a rather ominous sounding name. The purpose of this step in the design process is to analyze each transmission line in a design to insure that signal degradation from transmission line reflections, cross talk and ground bounce does not exceed the limits defined by the voltage levels in the Envelope of Allowed Values , as shown in Figure 1.

SIA uses electrical models for the output drivers, signal lines, connectors, inputs and any other components that are connected to a net. Using these models and analytical tools, such as SPICE, it is possible to calculate how each net will behave when very fast edge signals are sent down the net by the driver and detect cases where the signal has gone out of bounds. Figure 3 illustrates all of the signals on a clock net which has not been properly routed and terminated. It is clear that something will need to be done to improve this network if it is to function correctly in the finished PCB. This is the key value of Signal Integrity Analysis.

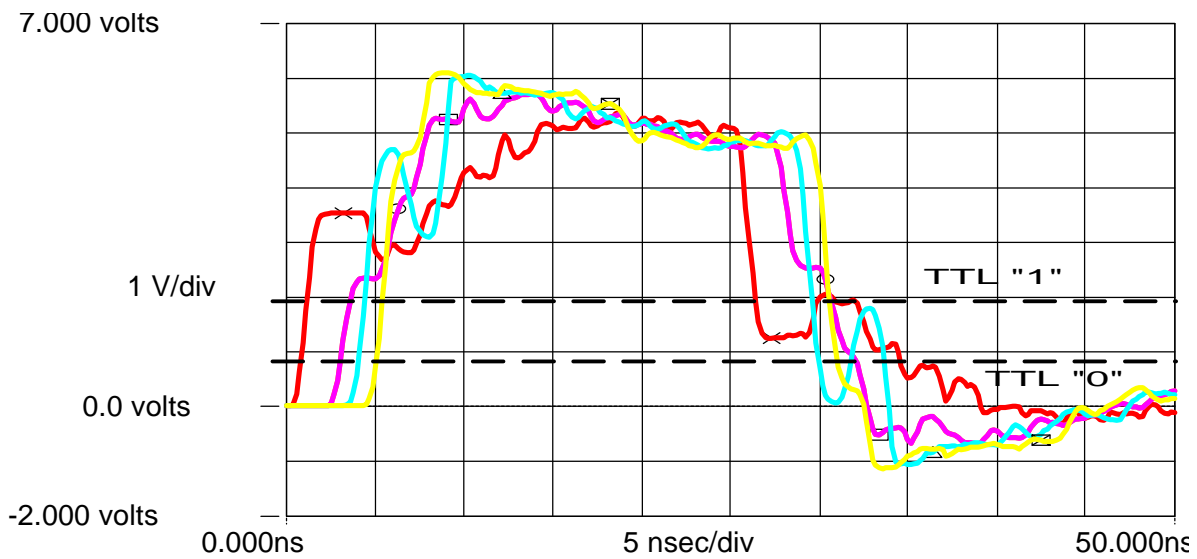


Figure 3. Simulation of a Clock Network using Signal Integrity Analysis

The Signal Integrity Analyzer block appears ahead of the routing step, which might cause one to ask how it is possible to do this simulation without actually routing the PCB. This is the place where it is desirable to do the analysis, because it allows problems to be corrected before the routing is completed. But, how is this possible?

The design flow leading up to the step is the secret to being able to perform SIA before routing begins. In order to perform timing analysis it was necessary to place all of the components in the final arrangement; connect the pins in the nets in the proper order to satisfy transmission line rules; and add terminations as appropriate. At this point, we can calculate the expected Manhattan length of each signal path and each wire in every

network. This means we have the complete topology of the net if it is routed to our rules. If we have established a cross section for our PCB and the spacing rules that will be used to route traces, we can calculate worst case coupling. This is precisely the information we need to do SIA and we can do it before we spend valuable time doing routing, enabling us to fix the problems and then reanalyze the design.

Consequences of Using Simulation and Analysis in PCB Design

The above discussion has implied that data is passed from one tool to the next. Indeed, for the process to work, organization of data and libraries must start at the schematic step in the process and then the design data be passed down to all later steps. Schematic capture packages designed to operate in this environment contain fields in the net list that allow the engineer to “tag” each net with a label or net attribute that informs all of the subsequent tools how to handle the net. This also implies that data is passed backward through some steps. These data exchanges are crucial to the success of the process. That is why the steps in the process must be tightly linked.

Linking the design steps requires that all of the tools used in the process are capable of using data from the other members of the set. The “easy” solution to this is to buy an integrated tool set from one vendor. This solves the interface problem and it is one of the selling points of integrated tool sets. The down side of these integrated tools sets is that none of them offer “best in class” tools for every step. As a result, most successful users purchase best in class tools for each step and do the interfacing themselves.

Throughout this article, statements have been made that suggest the tool used to route the PCB needs to be capable of following design rules. This is, perhaps, one of the most important changes that need to be made to the PCB design process. In order to insure that the signal integrity and timing rules established during the design process are preserved, the router must have the capability of recognizing the rules forwarded from earlier steps and then following them. Failing this, it is necessary to add a post-route analysis step to detect where the router has violated the rules and then back track to fix them.

In the design flow, post route analysis is shown as a step. In the context of this type of design flow it is meant to validate the routed result rather than to check on a poor routing operation. In most fully implemented design processes, this step is eventually skipped as confidence builds in the work done earlier. Of course, building confidence in the process and skipping this step adds value by reducing overall design time.

Other consequences of adopting the “right the first time” design process are that the user must acquire new skills, that there will be a substantial setup time to gather libraries, learn how to operate the systems and to interpret the results. These steps take time and make the first design through the process appear to take much longer than the traditional “design it, fix it and redesign it” process. However, the first design out of the process

has a high probability of being right and not requiring a respin. Subsequent designs come out even faster, require even less rework and, best of all, are far more stable when introduced into the factory.

Summary

A PCB design process that employs simulation and analysis to insure that each design has accounted for all of the variables in components and processing will produce far more successful designs in shorter times than conventional design methods. In order to successfully exploit the process and the tools, all of the members of the design process will need to acquire new skills and new design habits. Among competitors, the first to employ such disciplined design processes will be the most successful.

Perhaps the biggest benefit of the simulation and analysis design process is a hidden one. Design improvement results as a matter of course from the need to approach design with more discipline and the fact that it is necessary to provide the simulation and analysis tools with the complete set of information in order for them to do the job.

BIOGRAPHY OF LEE W. RITCHEY

7/25/97

Lee W. Ritchey, is Program Manager for common packaging at the Network Systems Operations of 3Com Corporation, a manufacturer of high performance communications network equipment. At 3Com he is in charge of high-speed design rule set creation for design of high performance switches, routers, com servers and hubs. He is a consultant to the various design groups on both high-speed design issues and EMI/RFI control. Part of his internal consulting at 3Com involves coordinating the packaging of all stackable networking products to insure common look and feel.

Ritchey was President of Shared Resources, Inc., a provider of PCB design services, high speed packaging engineering services and PCB design systems to major manufacturers of high performance computing equipment.

Prior to starting Shared Resources, Ritchey was responsible for manufacturing and test engineering at Magnuson Computers and was a member of the first engineering team at Amdahl Corporation. He was a co-founder of several Silicon Valley start-up companies.

Your instructor has more than 25 years experience in the packaging of high performance equipment ranging from microwave satellites to supercomputers, has been a member of the IPC Advanced Packaging Committee, and has served as a packaging engineering consultant to several developers of high performance computers, image processors and workstations. He is currently a member of the editorial review board of PCB Design Magazine and serves on the faculty of the PCB Design Conferences, teaching sessions on various high speed design topics.

A much-in-demand lecturer, Ritchey has presented courses in high-speed digital design at universities and design conferences around the world.