

Busses: What Are They and How Do They Work?

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Introduction

Webster's Encyclopedic Unabridged Dictionary defines a bus as "a motor vehicle with a long body equipped with seats or benches for passengers, usually operated as part of a scheduled service line." The Computer Engineering Handbook defines a bus as "the connection in a computer between the main memory and the processor that allows for the transfer of instructions and operands". The power distribution industry defines a bus as a set of very heavy conductors that tie circuit breakers together. All of these are examples of busses and all are intended to move large quantities of objects from one place to another. This article will focus on busses as they are used in the computing industry.

In the most general sense in electronics, a bus or data bus is used to move data words of any type from one place to another. Computing is based on data words made up of collections of data bits. These "words" can contain as few as four data bits and may have as many as 512 bits or even larger. (For a treatment of these bits and bytes, see "Bebop to the Boolean Boogie" by Clive Maxfield.)

The data bits in a word are ones and zeros represented by two voltage levels, one higher than the other. Usually the higher voltage or "logic high" represents a "logic one" and the lower voltage or "logic low" represents a "logic zero."

The task of a bus designer is to devise circuitry that passes these data words made up of a collection of highs and lows from one circuit to another. The least expensive method in terms of wire cost is to send the bits one at a time over a single pair of wires. This is called serial data transmission. Familiar examples of this are modem links, Ethernet connections and the assorted DSL connections used to connect to the Internet. Data words start as sets of bits that exist in parallel. In order to ship these words on a serial basis they must be converted to a serial stream of bits at the transmit end and then reconverted to a parallel word at the receive end. The common name for the circuitry that does this conversion is a Serdes circuit which stands for serializer/deserializer. At some point, it is more cost effective to add a wire for each bit in the word and send it in parallel on a "Bus".

Parallel Data Busses

Parallel data busses were the first types of data bus used in computers. They are also the most common types. There are several types of parallel data buses. The simplest is a unidirectional data bus with a single source and a single user or load. Figure 1 shows a four-bit data bus with clock.

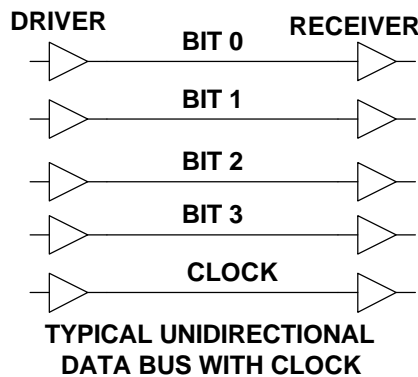


Figure 1. Unidirectional Four-Bit Data Bus With Clock.

These data busses can range up to 512 bits wide. Some places where unidirectional data busses are used are A/D and D/A converters and the address structures of memory arrays.

A more common form of data bus is a bidirectional data bus. Figure 2 shows a two point bidirectional data bus. In this configuration, data can be sent from either end. In order to insure that collisions don't occur as a result of both drivers trying to send data at the same time, some form of traffic management is needed. A bus supervisor circuit is used to insure only one driver set is active at once. The bus supervisor creates the clock signals required by both the driver and receiver circuit. The Northbridge and Southbridge ICs that are usually a part of a PC are examples of this type of function. This type of bus is commonly found in the data portions of memory arrays.

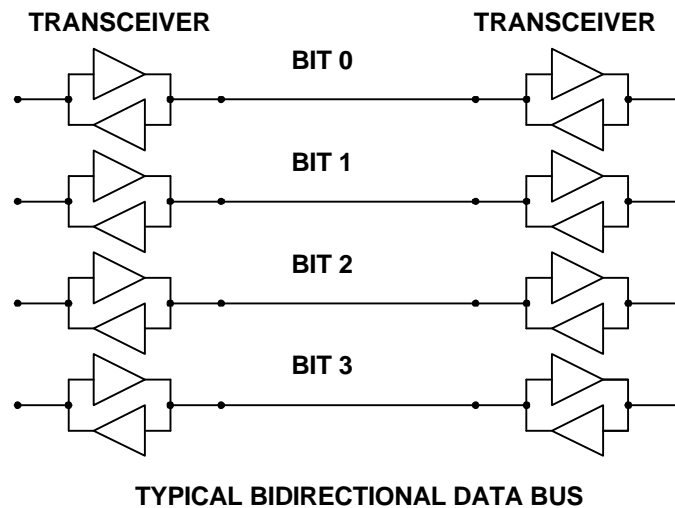


Figure 2. Bidirectional Four Bit Data Bus

Often, there are several sources and users of data that need to be connected to each other. Examples of this are the PCI and SCSI busses in a personal computer products or the VME bus that is found in a variety of instrumentation products. Such a busses have the loads and sources arranged along their length. These are known as a multidrop busses. The "drops" can be drivers only; receivers only or bidirectional connections. For any combination of these the control circuit must link them all together in such a way that conflicts referred to as bus contentions do not occur. Figure 3 shows one line in a bidirectional multidrop bus.

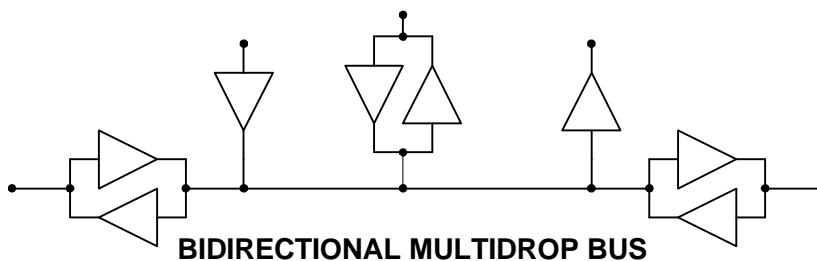


Figure 3, One line of a Bidirectional Multidrop Bus

As data busses become large, meaning they contain large numbers of bit lines, the space on a schematic required to show all of the lines becomes quite large. In order to simplify the creation of schematics, a shorthand method has been developed that substantially improves schematic readability. Figure 4 shows a 32 bit bus drawn with this shorthand notation. The bus is BUSABC and the numbers in the brackets indicate which data bits of the bus are shown in the connection. The line representing the multi-bit bus is drawn much wider or darker than a single signal line to indicate it is a bus.

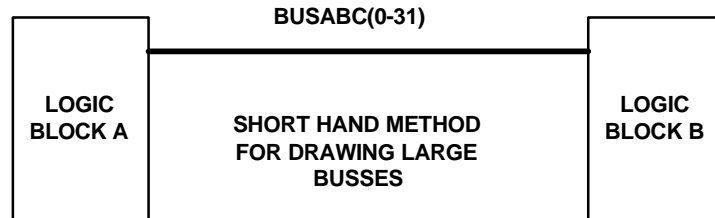


Figure 4. Shorthand Notation Method for Large Data Buses

Design Considerations for Buses

As can be seen in the examples given above, several data “bits” are sent from a source to a user all at once. On arrival at the user, the data is clocked into registers or other circuits that will operate on it. Clearly, layout must be done in such a way that all the bits arrive at the same time. This means that length matching will be required during PCB layout. The precision with which matching must be done is directly related to the data rate. The slower the data rate, the more time there is to wait for all bits to arrive allowing more length mismatch between bits in the bus. The faster the data rate, the smaller the time available to wait for bits to arrive resulting in a smaller budget for length mismatch among members of the bus.

As an example of length mismatch tolerance, the 33 MHz PCI bus has a period of 30 nanoseconds. Of this, more than two nanoseconds is available for length mismatch. At the speeds that signals travel in PCBs, this would allow members of the bus to be mismatched by up to 12 inches or 60 millimeters and still work properly. A 2.5 GB/sec data bus as is employed in the new Infiniband protocol has a period of only 400 picoseconds. The time available for length mismatches is only 60 picoseconds. This translates into a length difference of 300 mils or 7.5 millimeters.

In addition to managing length to insure timing is preserved among members of a bus, the designer must insure that proper terminations are used to match drivers and loads to the lines and insure that loads are spaced such that their loading does not degrade signals excessively. Each of the bus specifications defines how this must be done.

Types of Parallel Buses

There are several parallel bus “standards” in wide use in computer and instrumentation design. Among these are the Personal Computer Interface of PCI bus, SCSI or Small Computer Systems Interface bus, the Compact PCI bus, the VME bus used in instrumentation, the Rambus interface used in very high performance memories, and others. The web sites for some of these are listed at the end of this article.

Parallel busses have a limited data rate at which they can be reliably run. In most cases this is 225 megabits per second per line. When higher data transfer rates are needed, more lines are placed in parallel. When bus widths reach 128 lines, the noise transients associated with all lines switching from zero to one or one to zero can limit the length of the bus to an unusable dimension.

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Types of Serial Busses

The cause of the switching transient problem in parallel busses is traceable to the current transients needed to charge up all of the single ended lines or discharge them. This is called simultaneous switching noise. A solution to this problem is to use differential signaling. In this protocol, each data bit is sent on a pair of lines with one line going positive while the other goes negative. In this way, the net current flowing in the "ground" portion of the circuit is zero and the noise problem is dramatically reduced. References 1, 5, 6, & 8.

Beginning with the **Firewire** (1394) peripheral bus devised by Apple Computer, differential signaling has found its way into a host of products that would not function properly if dependent on the single ended switching common to most parallel busses. Among the protocols available are:

LVDS- Low Voltage Differential Signaling first devised to allow data transfer from laptop mother boards to flat panel displays.

Fiber Channel- a differential signaling protocol used to connect disc drive arrays together. Data rates as high as 1 gigabit per second are possible.

Infiniband- a full duplex differential signaling protocol intended to replace the PCI bus in PCs and servers. Data rates as high as 2.5 gigabits per second are possible.

Conclusion

Data busses are the work horse of digital signaling. They are how components of logic based products are connected to each other. Data bus protocols exist to meet a broad range of performance and cost targets. Design specifications are maintained for all of the common bus protocols. These specifications contain the design and performance rules needed to use them successfully. Most of these specifications are accessible from public web sites.

Web addresses for several newer bus protocols:

www.Infinibandta.org- Infiniband bus specification. Replaces PCI bus in PC based products.

www.RapidIO.org- RapidIO bus specification.

www.usb.org- USB implementers forum.

www.1394ta.org- 1394 bus specification, also referred to as Firewire.

www.rambus.com- Rambus Memory specification

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