



ONE DAY COURSE

GETTING TO 32 Gb/S, HOW TO DESIGN VERY HIGH SPEED DIFFERENTIAL PAIRS

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This one day course is intended to cover all of the technical issues involved in the design of very high speed differential pair signal paths. This is a thorough treatment of all of the topics that must be considered in order to be successful as the speeds of differential pair signal paths continue to increase.

28Gb/S signaling is already being successfully shipped in high performance servers, routers and switches. When data rates exceed 5 Gb/S there are a number of areas that need to be managed which were not significant issues at lower data rates. Among these are the type of glass weave used in laminates, the surface finish on the copper used for signal layers and the loss characteristics of the laminate itself. Effects of vias and other drilled holes can have a significant effect on signal quality if not properly managed.

This course will draw on more than 30 test PCBs built to determine the properties of new laminate systems as well as to measure the effects of vias, plane crossings and other features that might affect high speed signals.

TOPICS INCLUDE:

- How differential pairs operate
- Power delivery issues with differential pairs
- Managing cross talk in differential pairs
- Signal degradation sources- a real data path will be modeled and signal speed increased
- Bandwidth requirements for differential pairs
- How skew affects differential pairs
- How laminate choices affect skew
- Managing skew in differential pairs
- How laminate choice affects loss
- How choice of copper finish affects loss
- How processing at fabricators affects loss
- Routing differential pairs for optimum performance
- Choosing connectors for high speed differential pairs
- Connector pin out to minimize unwanted cross talk
- How vias can affect signal quality
- When can vias be ignored?
- How to prevent vias from degrading signal quality
- Choosing materials that enable good signal quality without over specifying
- Is a low DK (dielectric constant) material necessary for high speed signaling?
- Handling high speed differential signals on twisted pairs
- Handling high speed differential pairs on flexible circuits
- Characteristics of new laminates developed for high speed signaling
- Adaptive transceivers
- Equalizing techniques
- Simulation of high speed data paths
- Documentation required in order to insure boards containing high speed differential pairs are properly fabricated

WHO SHOULD TAKE THIS COURSE

This course is designed for all of the participants in the design process. Among those who will find this course valuable are:

- Design Engineers
- System Architects
- EMC Specialists
- Signal Integrity Engineers
- Technicians
- PCB Layout Professionals

- Applications Engineers
- IC Designers
- IC Packaging Engineers
- Test Engineers
- Project Engineers
- Design Engineers
- Engineering Managers

WHY TAKE THIS COURSE

As the speeds of high data rate serial links continues to increase, the margins for error and loss continue to decrease. In order to manufacture PCBs that perform properly at these ever increasing data rates far more control over materials, manufacturing and layout is necessary. This course covers each of these crucial areas in enough detail to assure successful first time designs.

PREREQUISITES

It is useful to have completed the two or three day signal integrity course offered by Speeding Edge, but not necessary. Good engineering training is also valuable, but PCB designers will get valuable information from the course that will enable them to understand why new layout requirements have been added to their tasks.

MATERIALS PROVIDED TO STUDENTS

Each student will receive a binder with all of the class slides in it. In addition, a CD with a large collection of pertinent articles and technical papers will be provided that will be loaded onto a server accessible to each student for downloading.

For information on scheduling this course contact:

www.speedingedge.com

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